

Compal Confidential

PEW76/86/96 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-07-20

LA6552P REV: 1.0

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Model Name : PEW96

File Name : LA-6552P

P/N : DA60000IM10

PCB

ZZZ

LA-6552P RE1 MB

LA-6552P MB Rev0: DA60000IM00

LA-6552P MB Rev1: DA60000IM10

LA-6552P MB Rev1: DAZ0FQ00200

Danube

AMD SIG4 Processor

uPGA-638 Package

Champlain page 6,7,8,9

Memory BUS(DDR3)

Dual Channel

1.5V DDRIII 1066~1333MHz

204pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3

page 10,11

Hyper Transport Link

16 x 16

ATI RS880M

uFCBGA-528

page 12,13,14

A link Express2

Gen1

ATI SB820M

uFCBGA-605

page 18,19,20,21,22

Thermal Sensor

ADM1032

page 8

LVDS

page 15

CRT

page 17

HDMI Conn.

page 16

MINI Card 1

WLAN

page 26

GPPI

LAN(GbE)

Broadcom

BCM57780

page 24

GPPI0

RJ45

page 25

LED

page 29

Fan Control

page 32

RTC CKT.

page 18

LID SW / MEDIA/B

page 28

Power On/Off CKT.

page 32

DC/DC Interface CKT.

page 33

Power Circuit

page 34,35,36,37,38
39,40,41,42

Extend Card/B

1. USB X2

2. ODD X1

Touch Pad

page 29

Int.KBD

page 29

EC I/O Buffer

page 29

BIOS

page 29

LPC BUS

ENE KB926

page 28

SATA HDD

Conn. page 23

port 0

SATA ODD

FFC Conn. page 23

port 1

S-ATA

Gen2

3.3V 48MHz

3.3V 24.576MHz/48Mhz

HD Audio

USB port 0,1,2

USB port 5

Bluetooth Conn

<Option> USB port 7

Mini card (WL)X1

USB port 8

Card Reader

RTS5137

USB port 6

HDA Codec

ALC272X

page 30

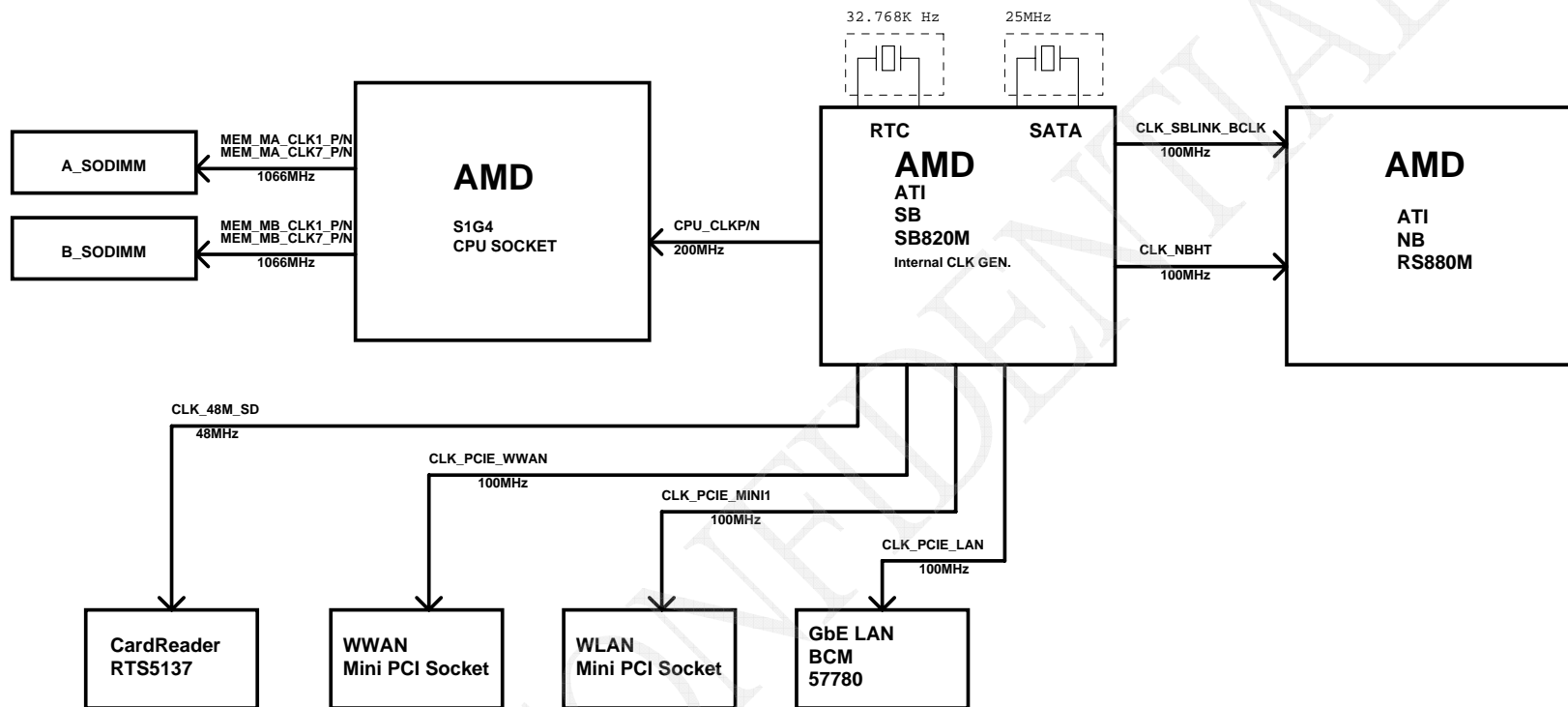
Audio AMP

page 31

Phone Jack x2

page 31

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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (1.375-1.5V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+CPU_VDDR	1.05V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V power rail for MINI Card	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

SB820
SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2		
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB820
SM Bus 1 address

Device	Address
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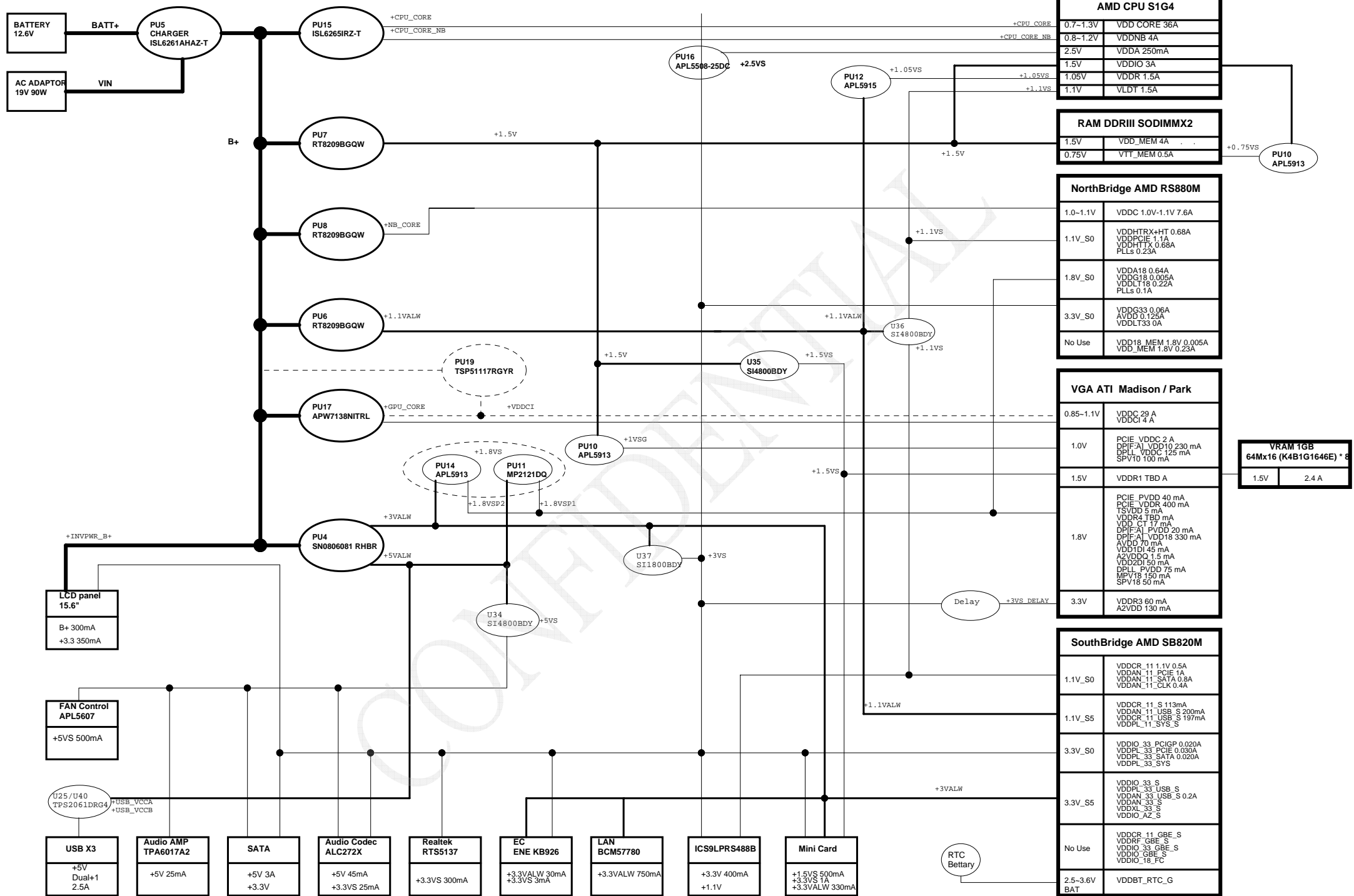
Board ID / SKU ID Table for AD channel

BOARD ID Table

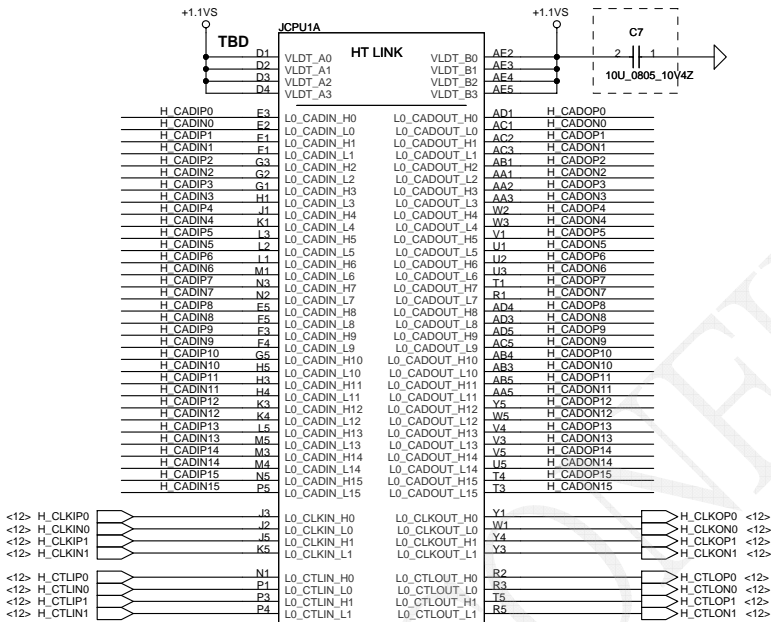
BTO Option Table

Project ID Table

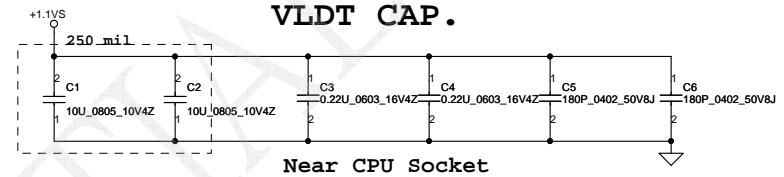
Board ID	PCB Revision
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1	PEW76/86/96
2	
3	
4	
5	
6	
7	



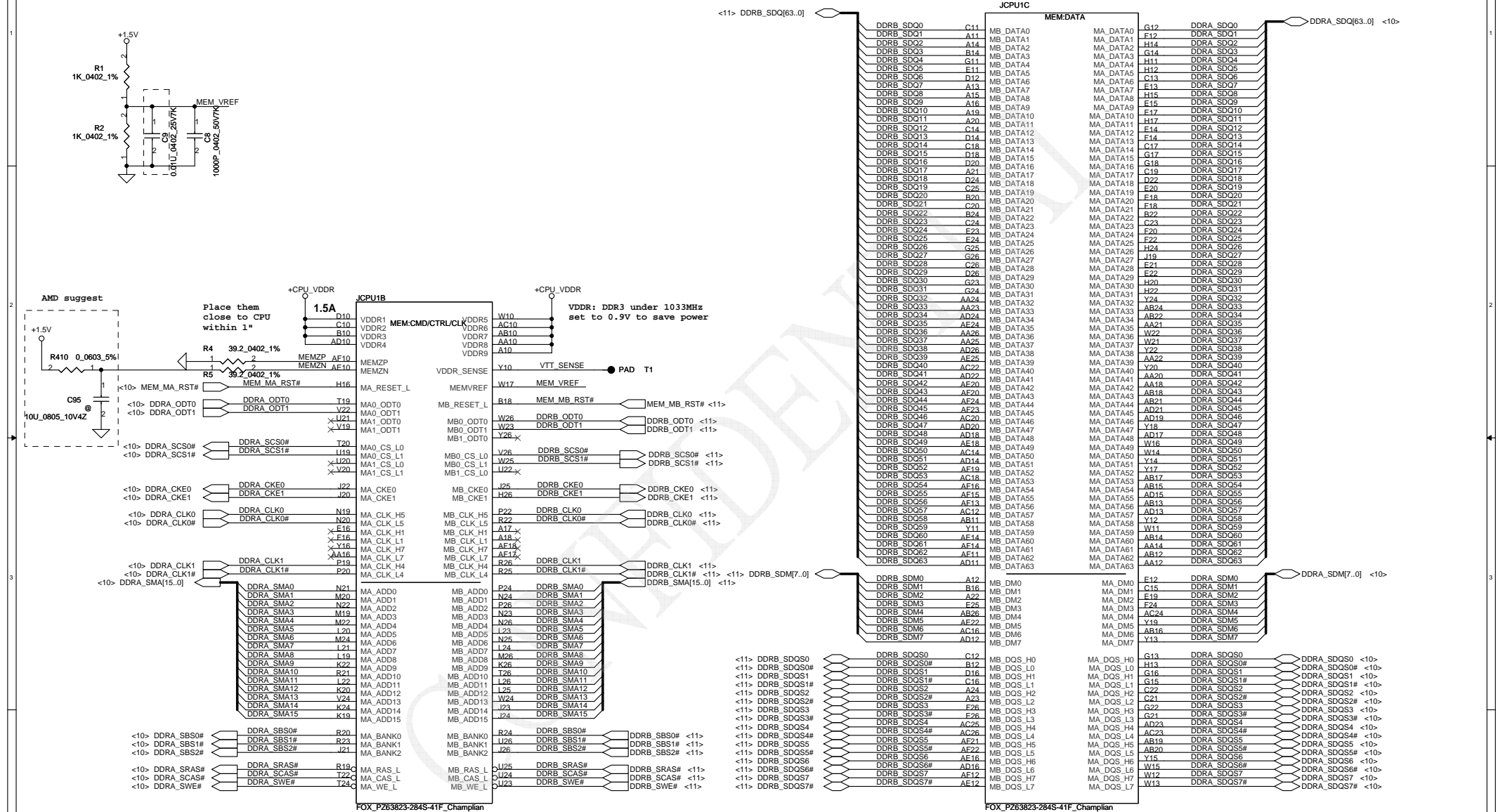
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FOX_P263823-284S-41F_Champian



Processor DDR3 Memory Interface

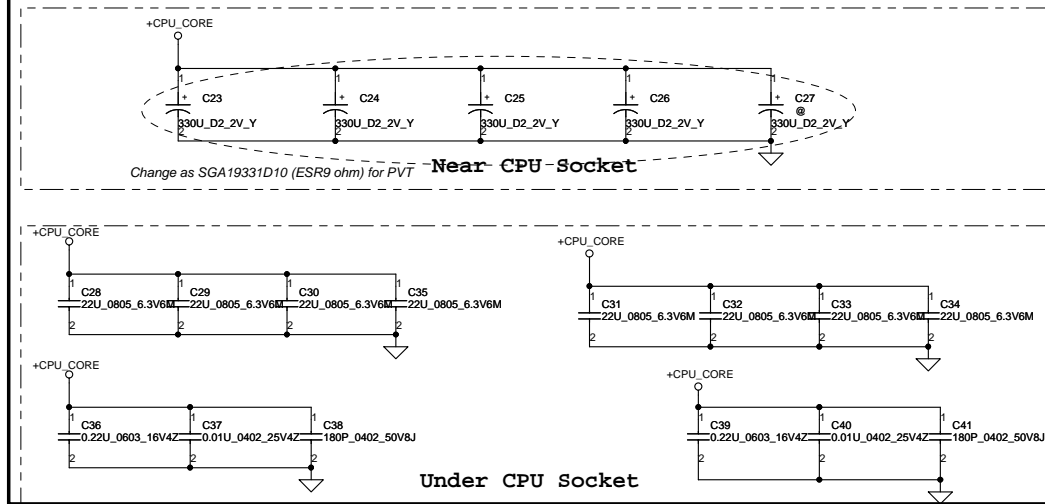


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				AMD CPU S1G4 DDRIII I/F			
				Document Number PEW/76/86/96 LA-6552P			
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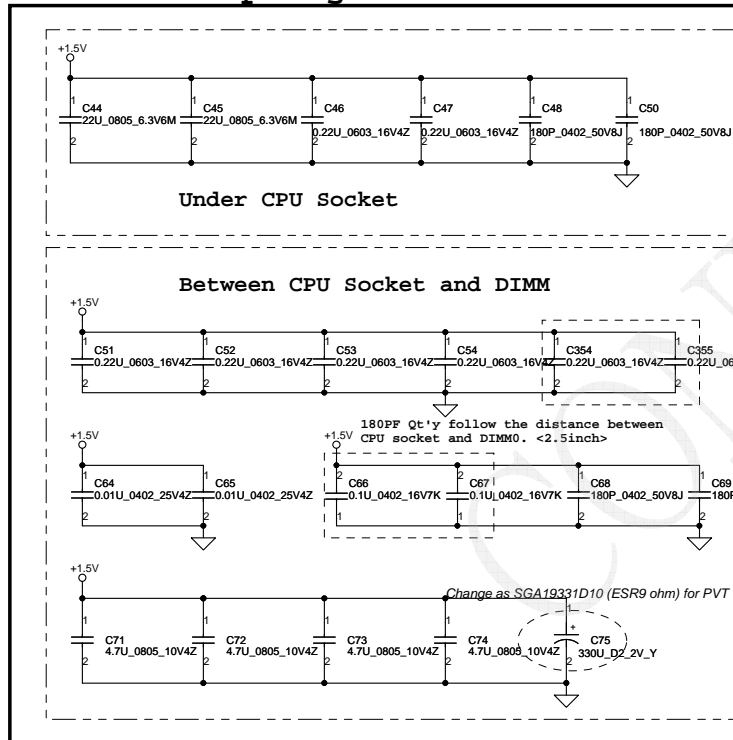


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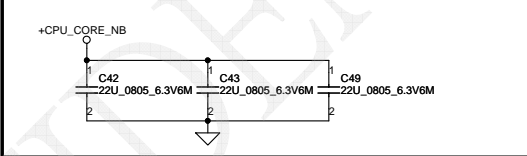
VDD(+CPU_CORE) decoupling.



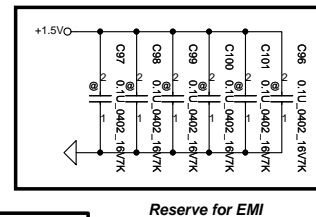
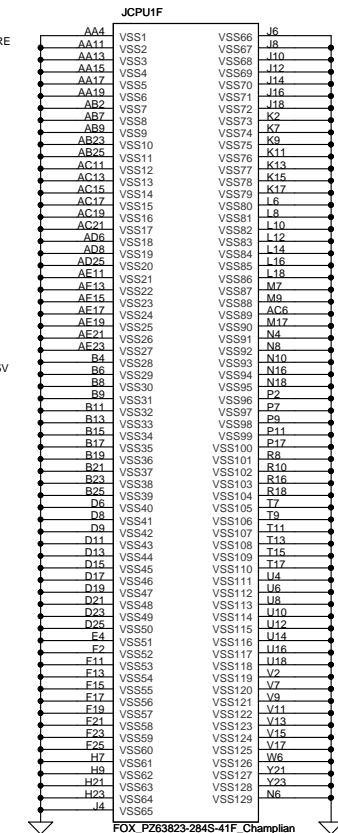
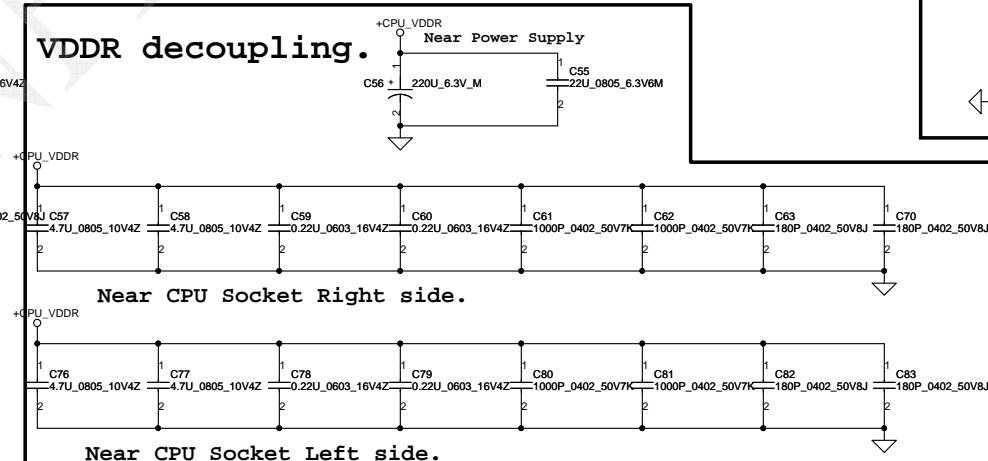
VDDIO decoupling.



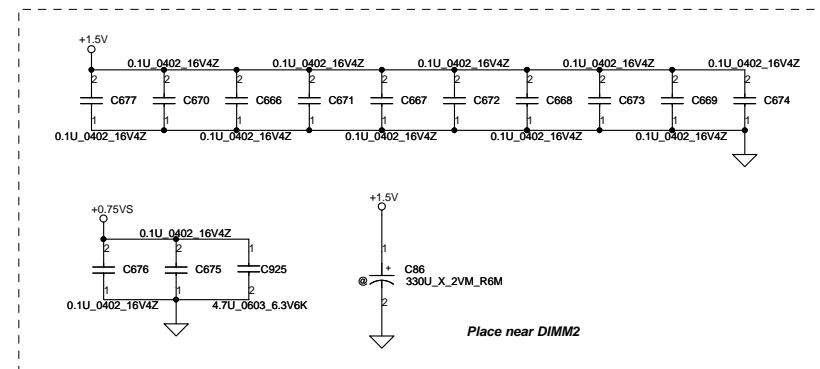
+CPU_CORE_NB decoupling.



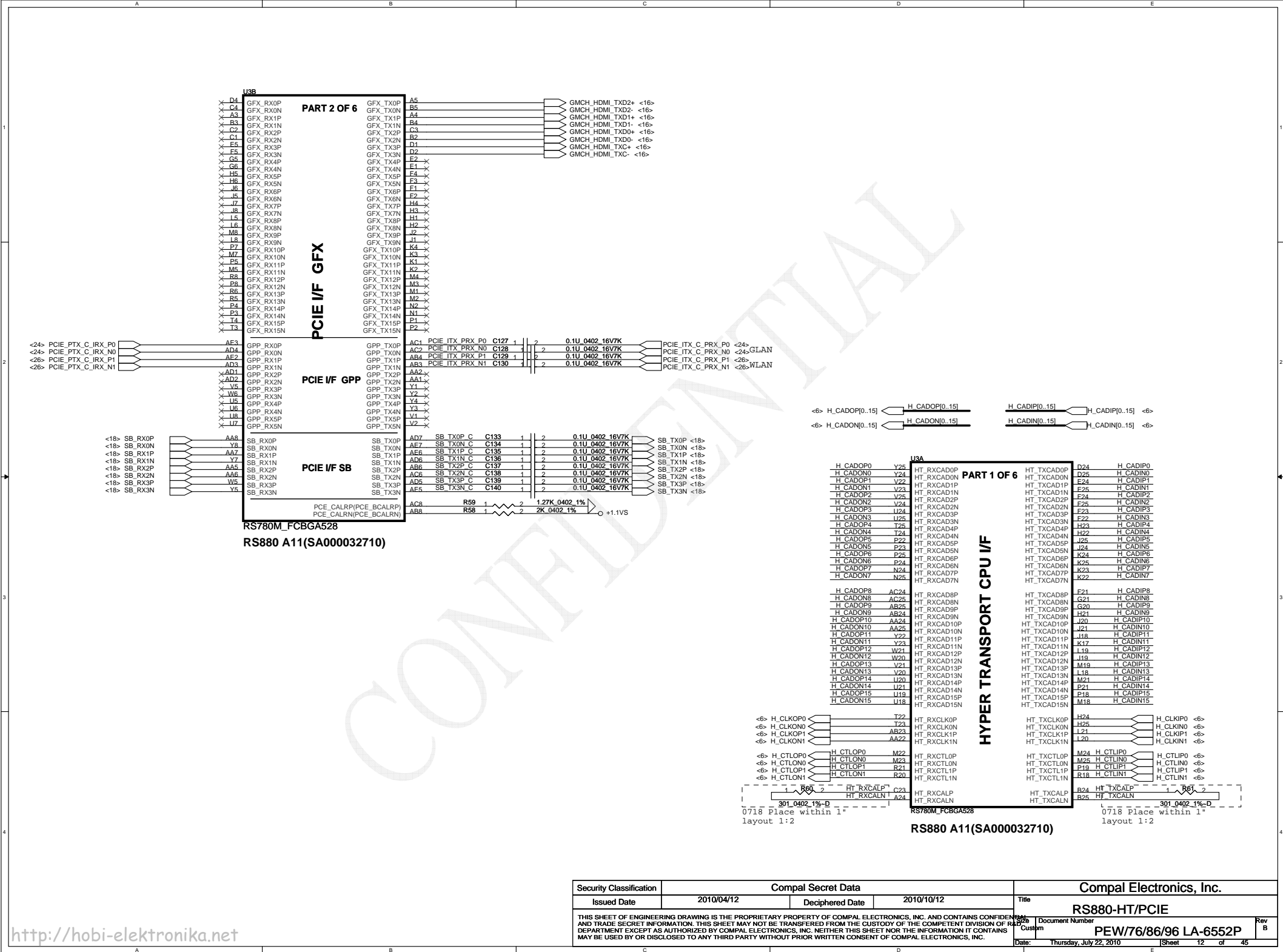
VDDR decoupling.



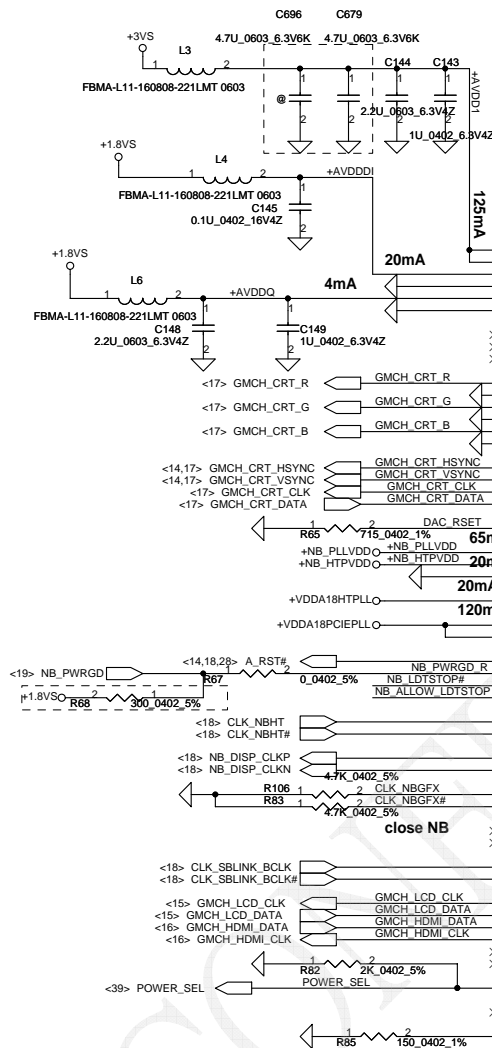
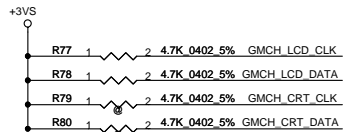
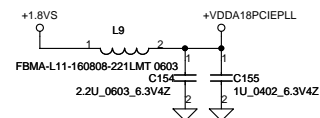
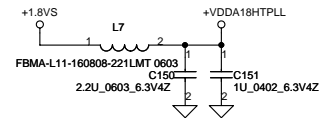
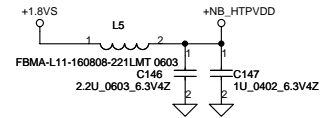
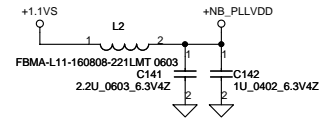
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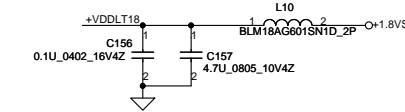
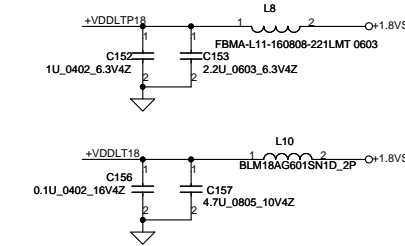
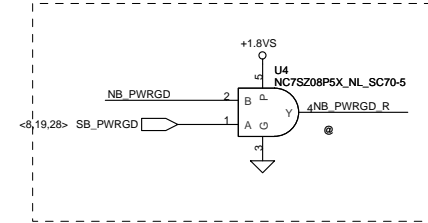
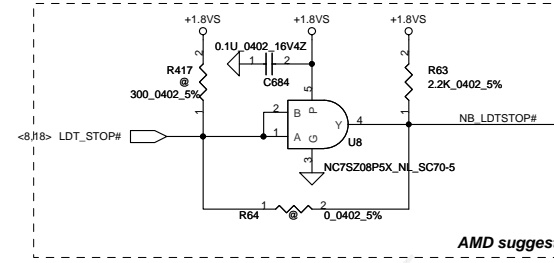
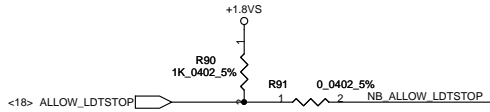
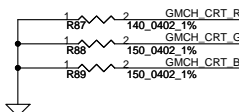
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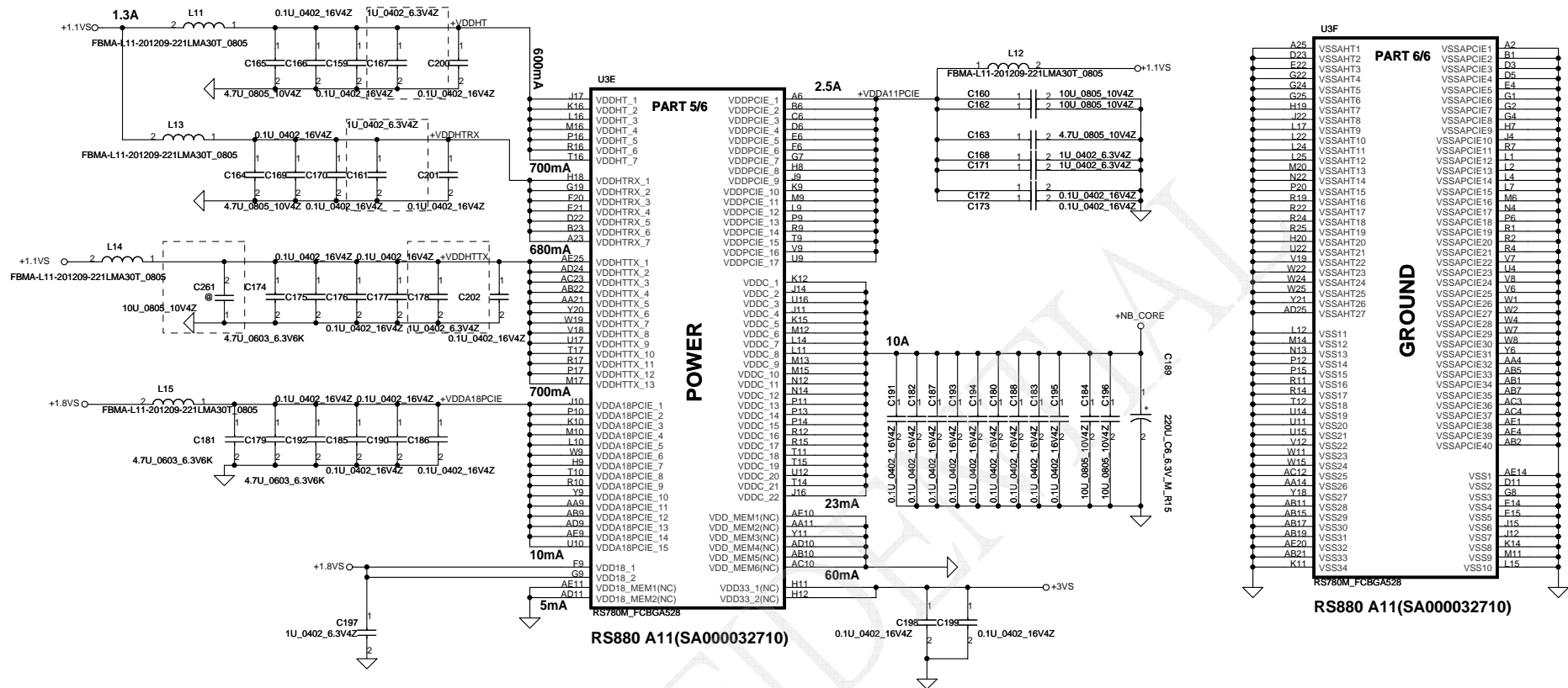
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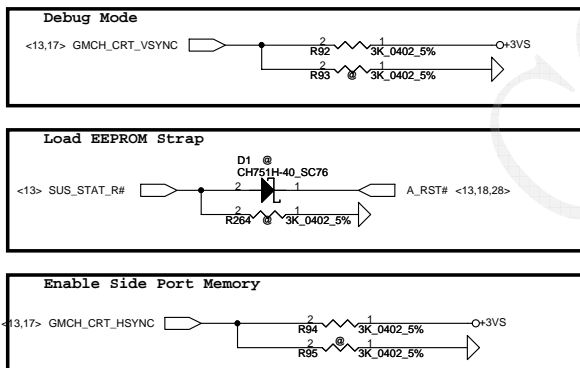
RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V



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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEB

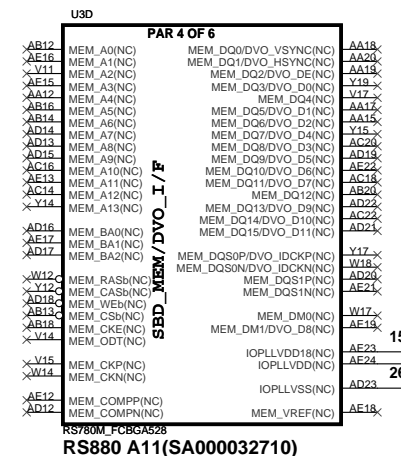
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

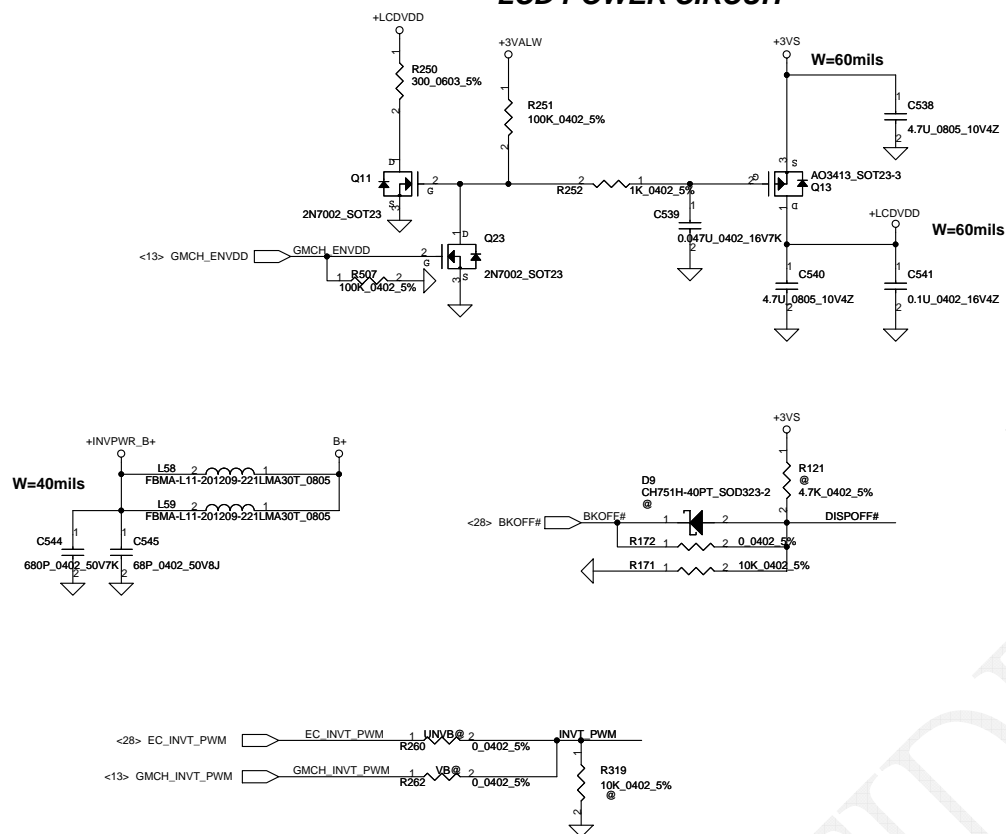
Enable Side Port Memory

RS880: HSYNC#
0 : Enable
1 : Disable
Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]

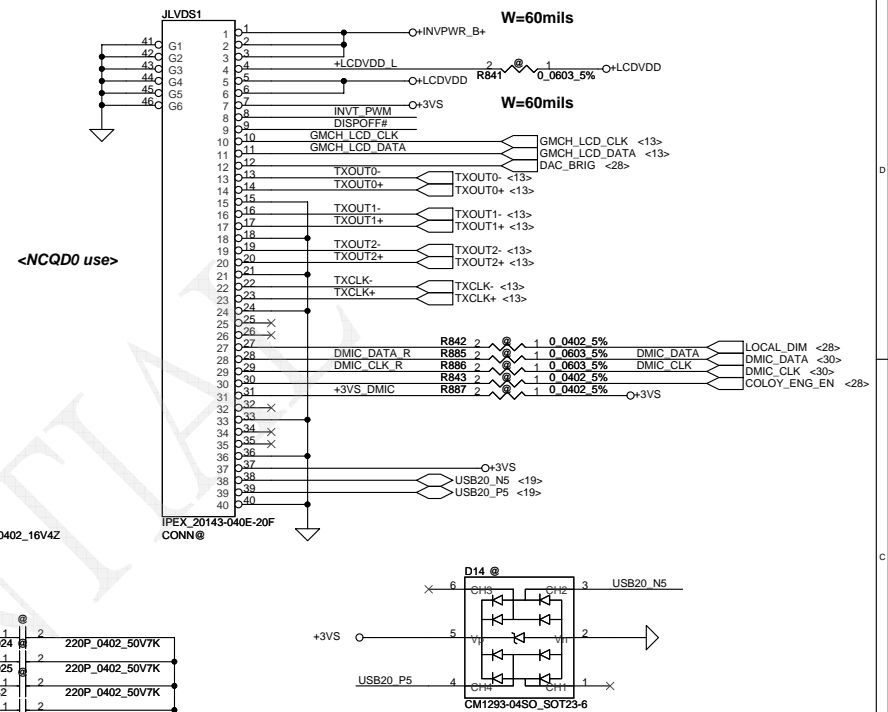


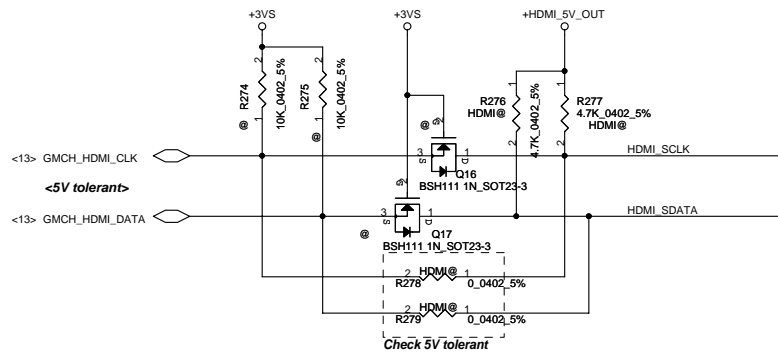
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LCD POWER CIRCUIT

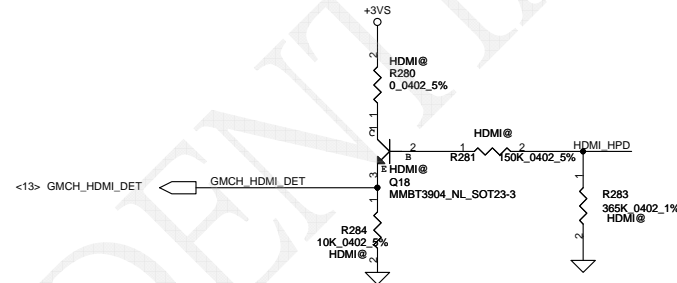
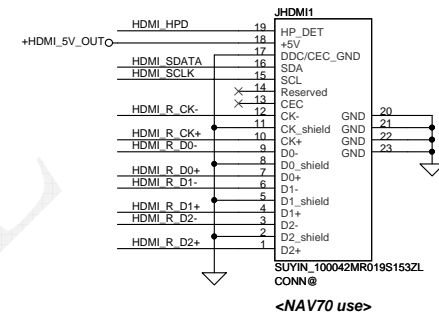
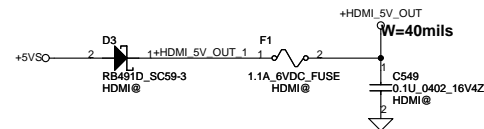
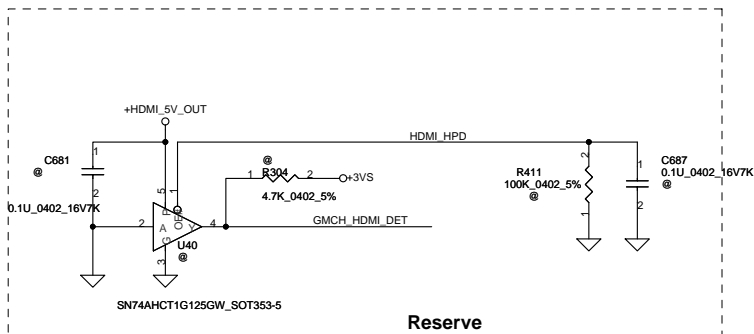


LCD/LED PANEL Conn.

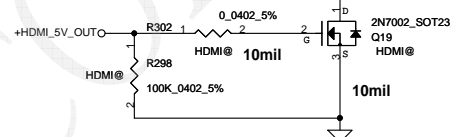




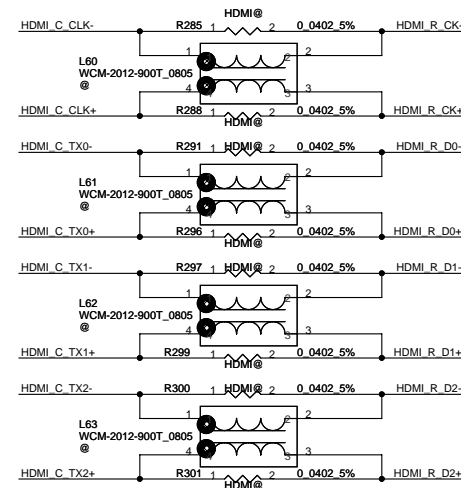
Place closed to JHDMI1



<12> GMCH_HDMI_TXD2-	C550	HDMI@	1	0.1U_0402_16V7K	HDMI_C_TX2-	R286	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD2+	C551	HDMI@	1	0.1U_0402_16V7K	HDMI_C_TX2+	R287	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD1-	C552	HDMI@	1	0.1U_0402_16V7K	HDMI_C_TX1-	R289	1	HDMI@	2	715_0402_1%
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<12> GMCH_HDMI_TXD0-	C554	HDMI@	1	0.1U_0402_16V7K	HDMI_C_TX0-	R292	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXD0+	C555	HDMI@	1	0.1U_0402_16V7K	HDMI_C_TX0+	R293	1	HDMI@	2	715_0402_1%
<12> GMCH_HDMI_TXC-	C556	HDMI@	1	0.1U_0402_16V7K	HDMI_C_CLK-	R294	1	HDMI@	2	715_0402_1%
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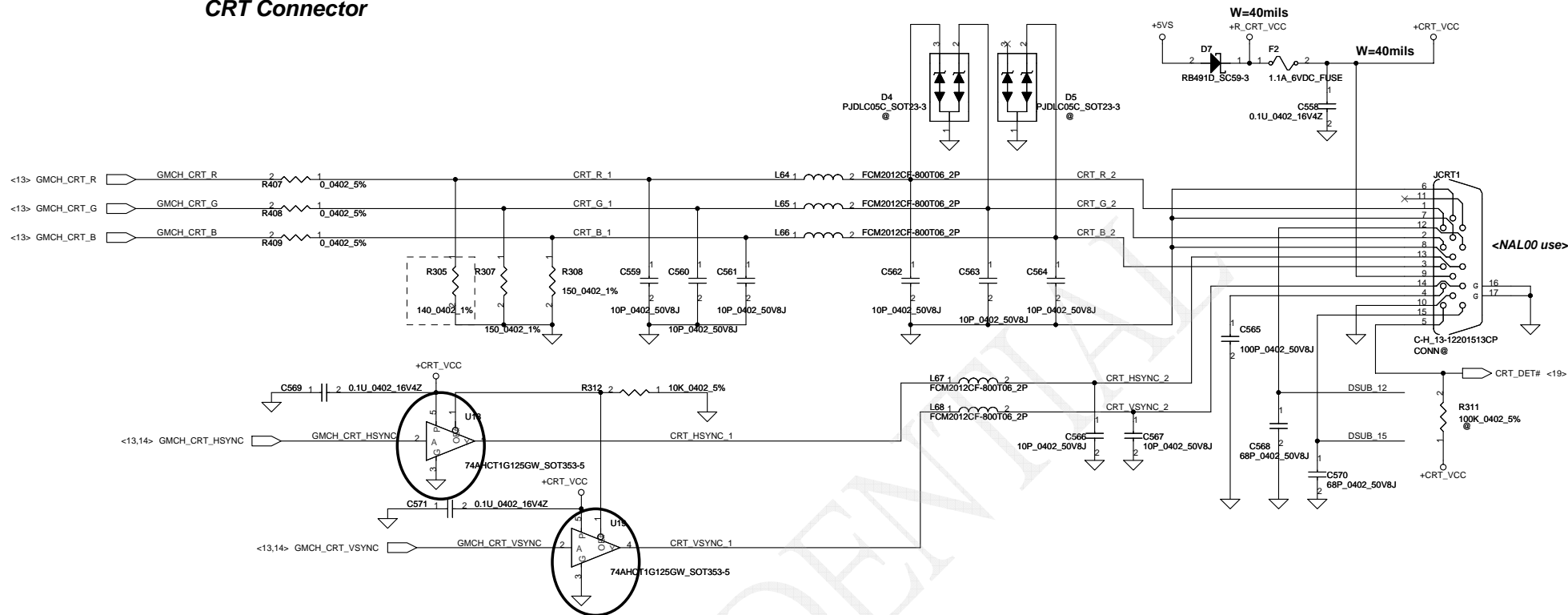


Place closed to JHDMI1



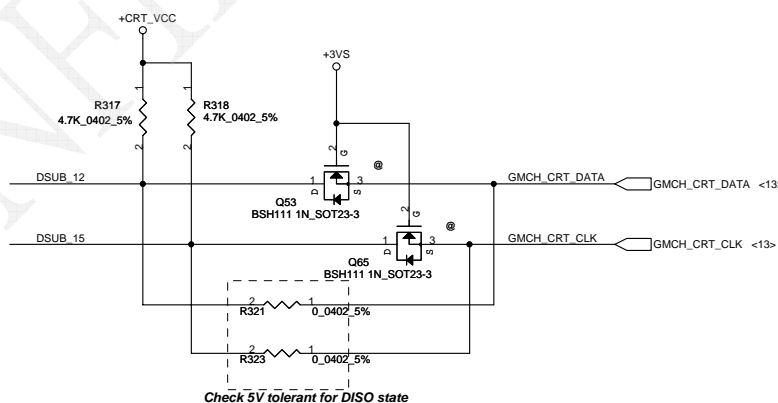
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CRT Connector

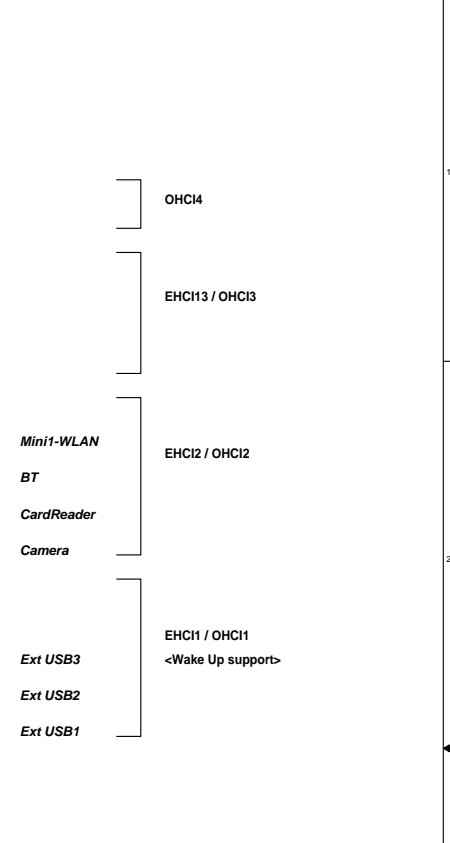
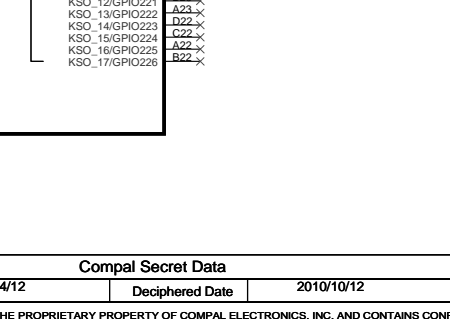
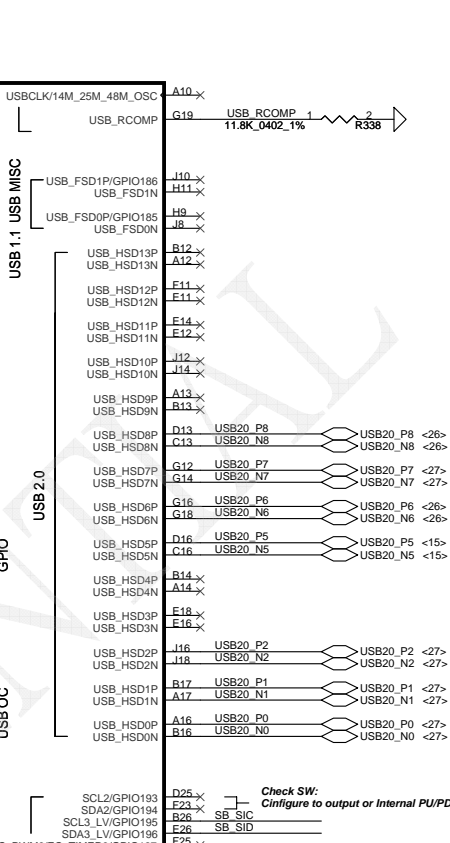
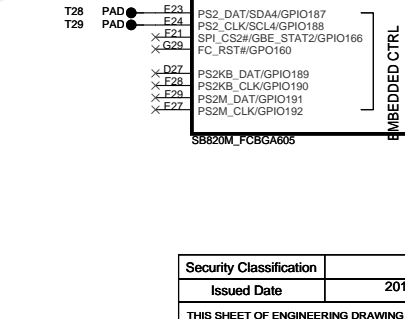
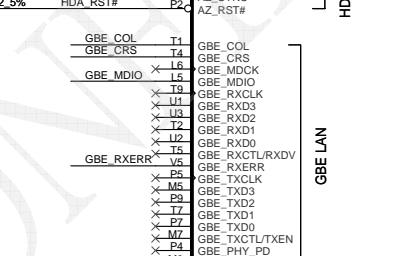
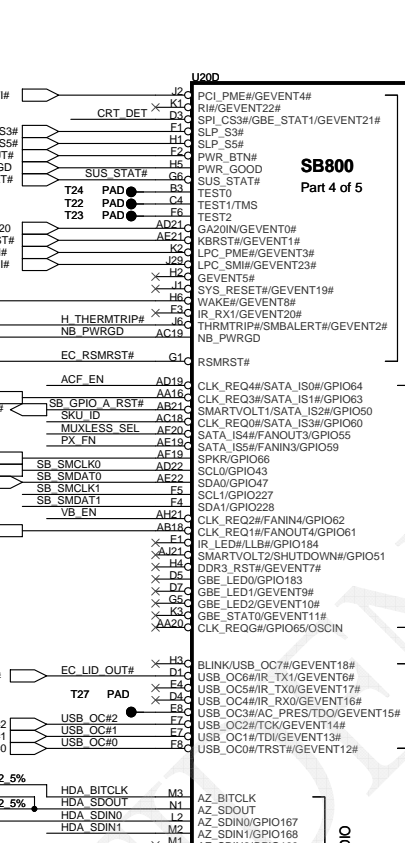
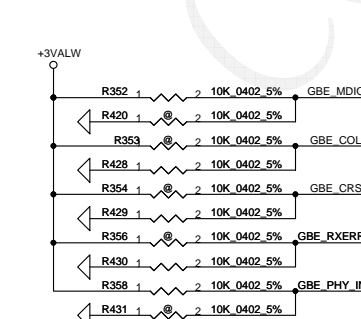
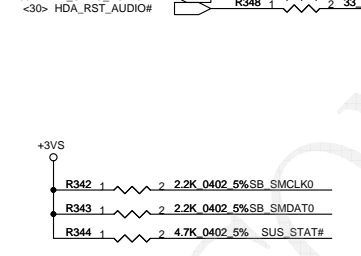
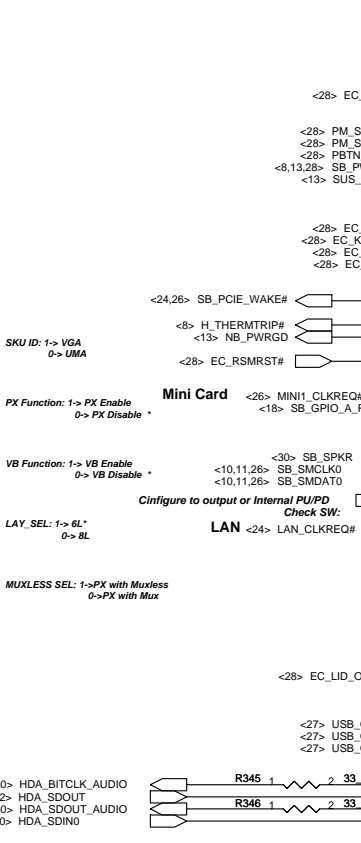
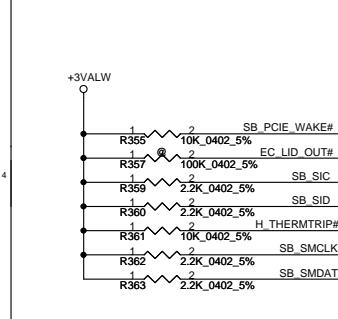
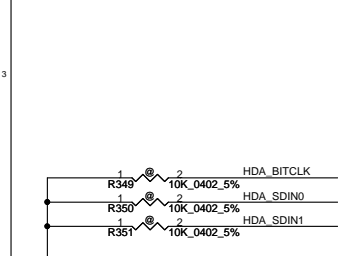
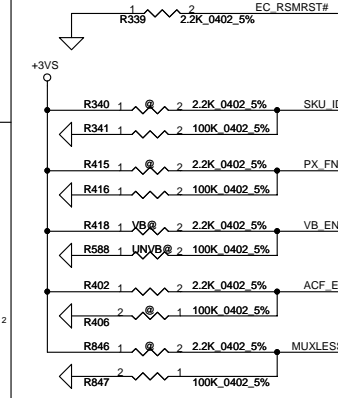
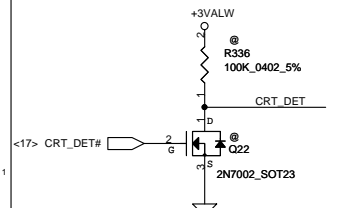


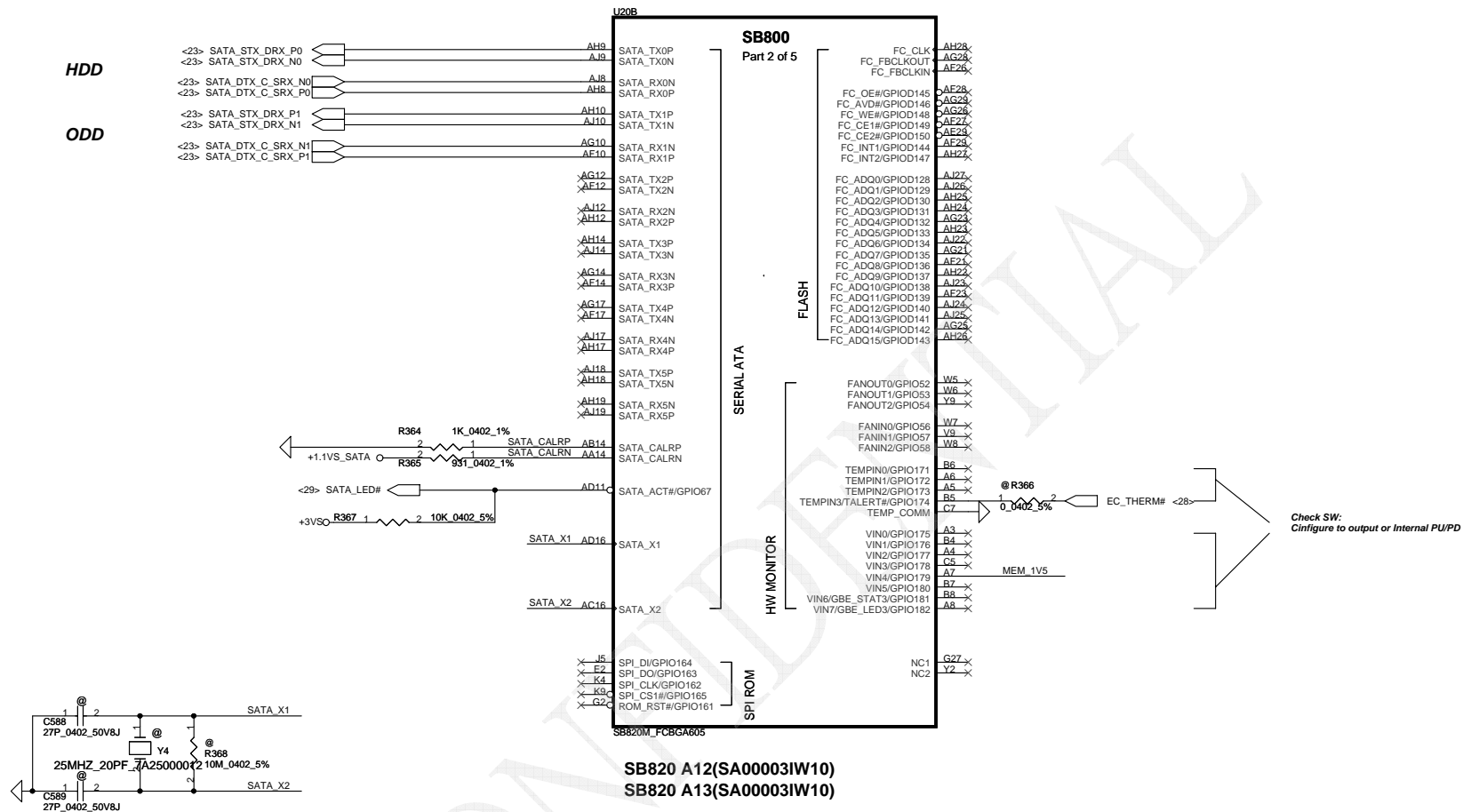
Change as SA411250110

Close to Conn side

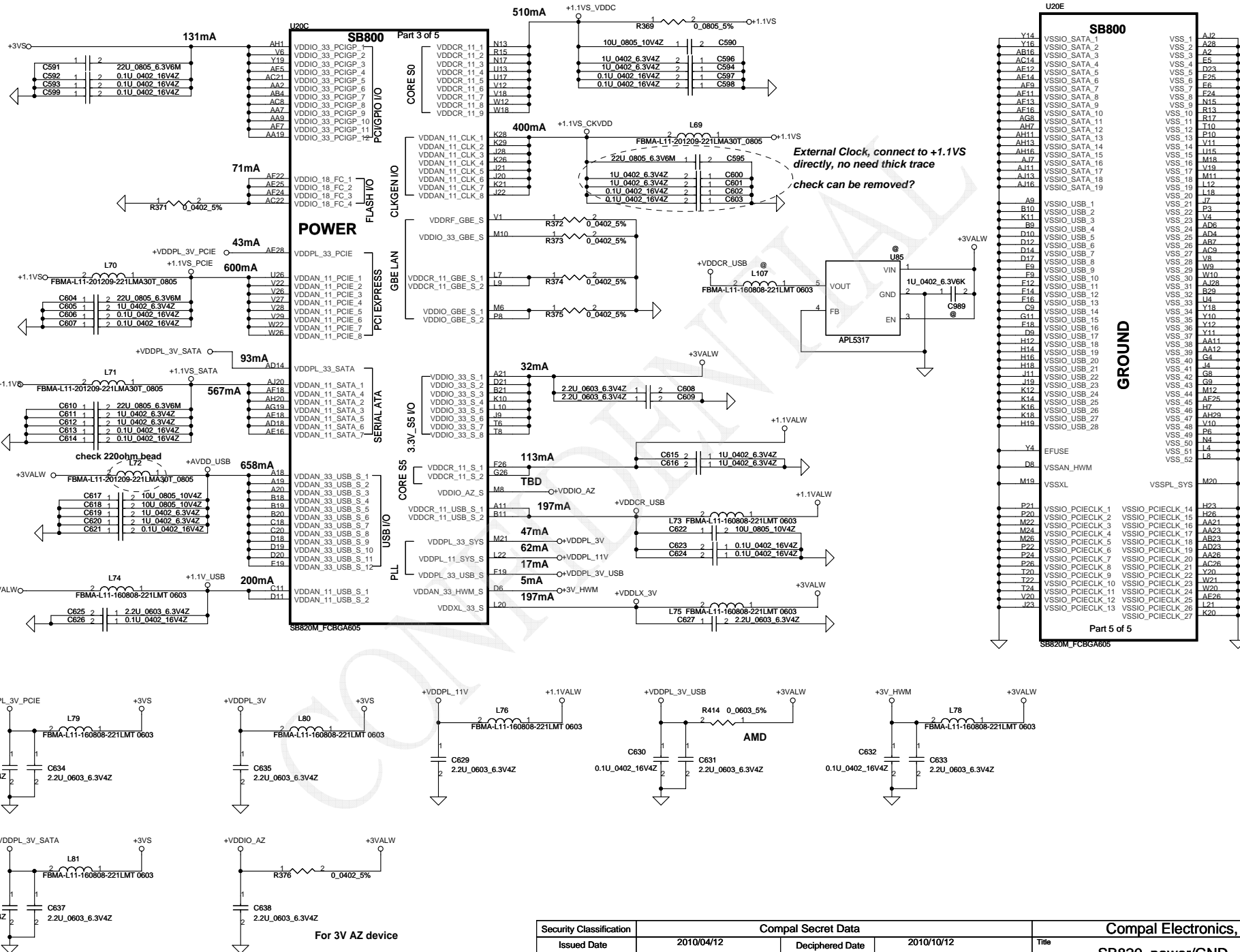


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				Date: Thursday, July 22, 2010	Sheet 20 of 45

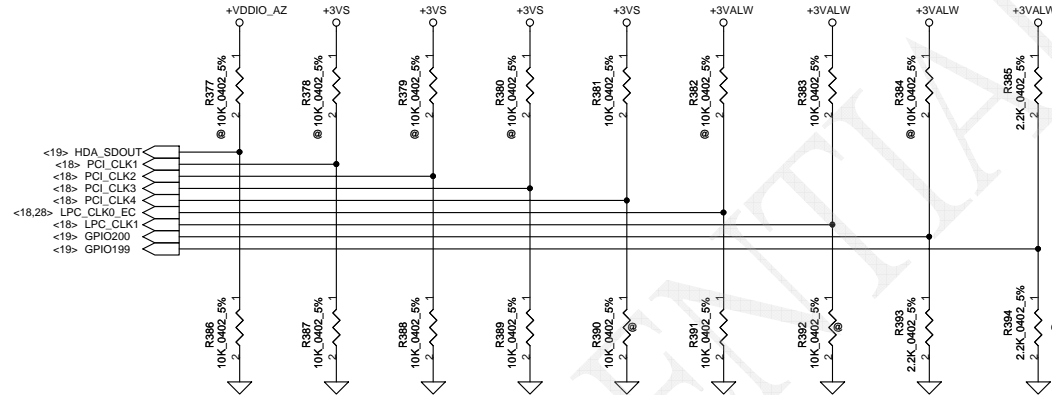


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										Custm		PEW/76/86/96 LA-6552P			
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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE		L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT			



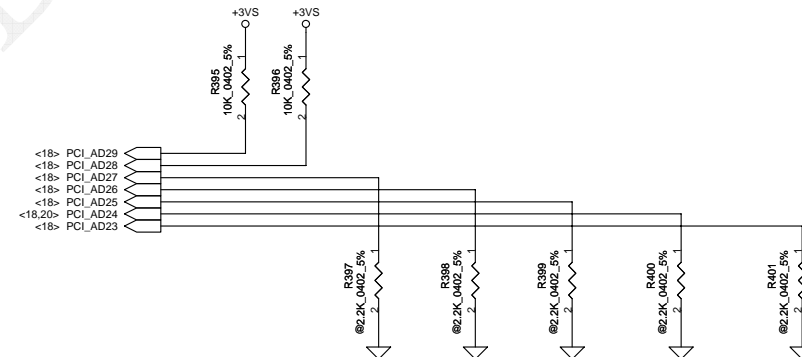
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

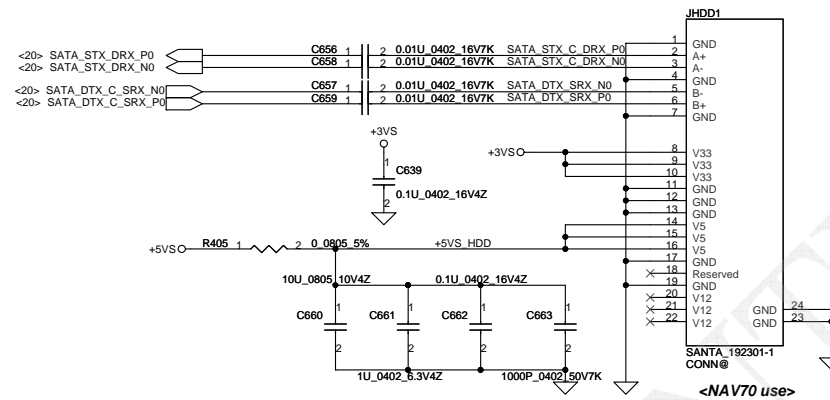
		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

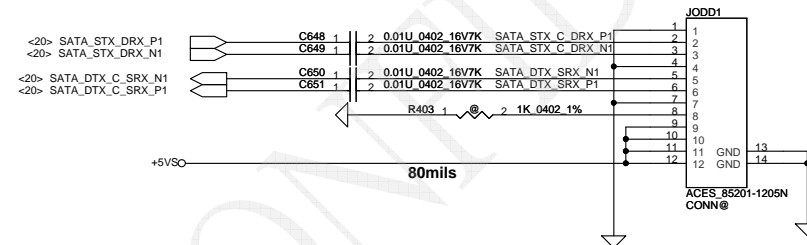
check default

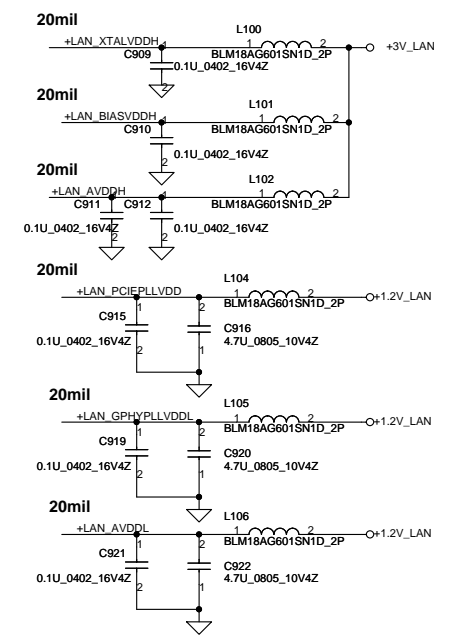
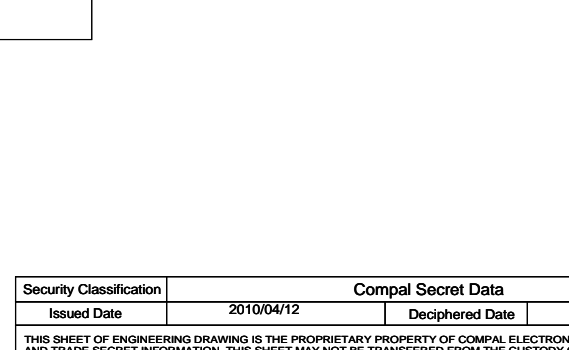
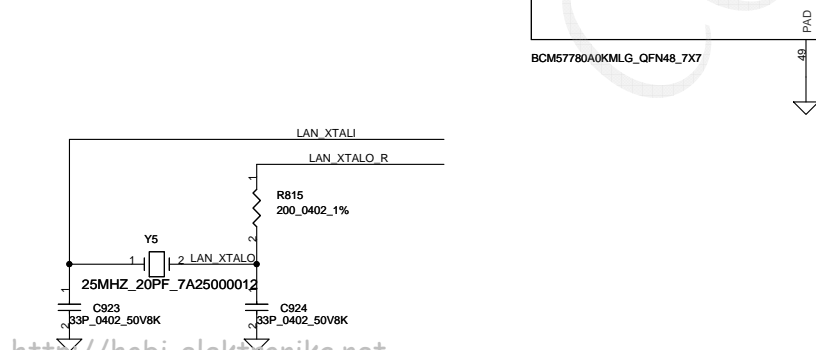


SATA HDD Conn.



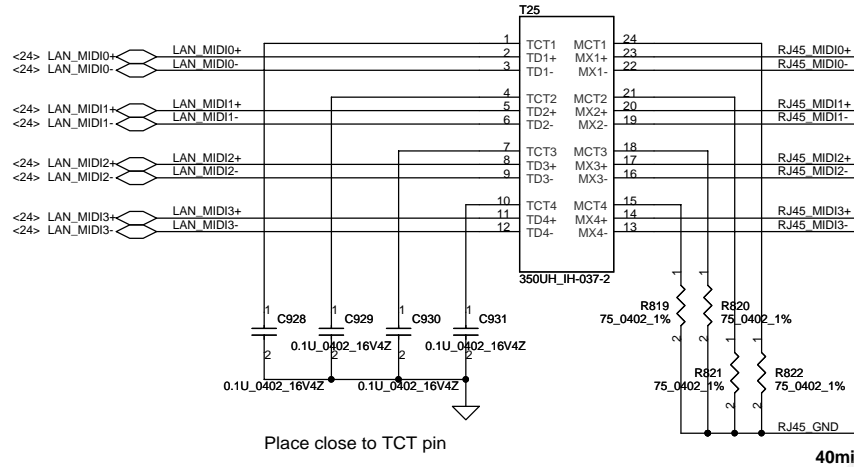
SATA ODD FFC Conn.



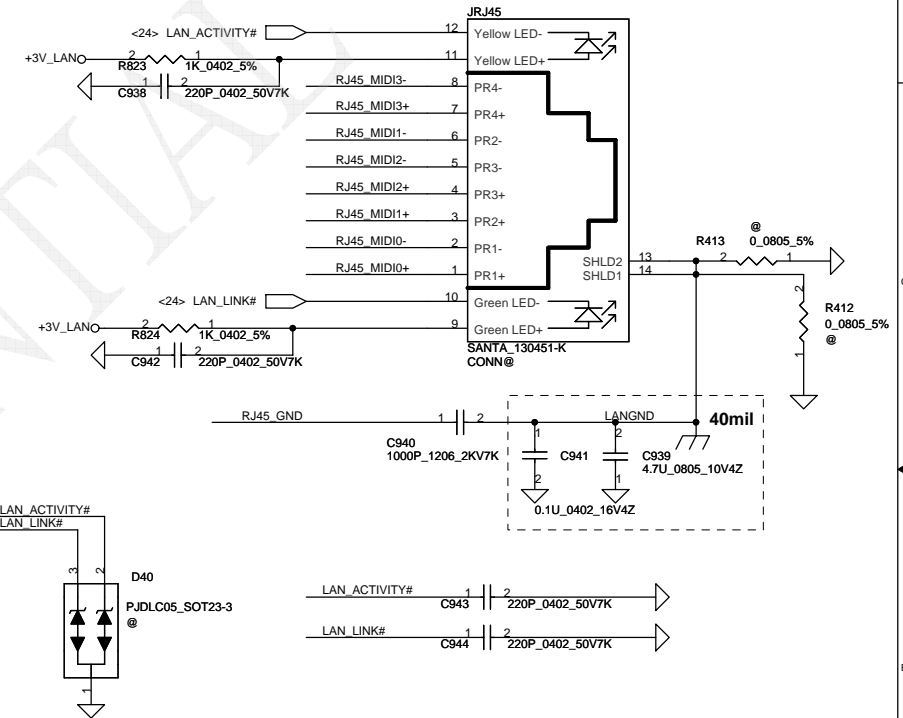


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				Document Number			
				Date:	Thursday, July 22, 2010	Sheet	24 of 45

BH GS5009-D <SP050006B00>

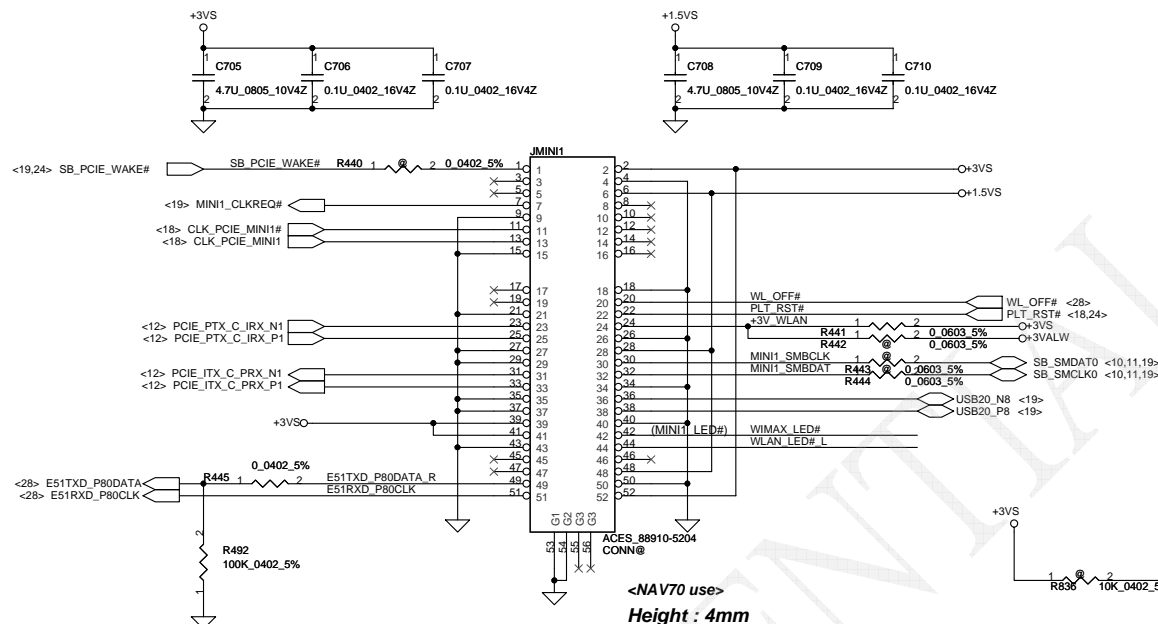


LAN Connector

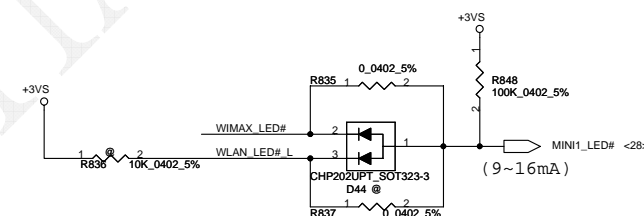


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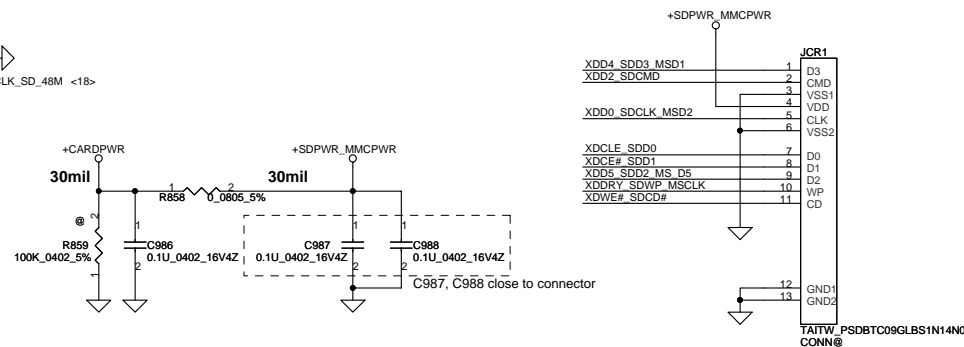
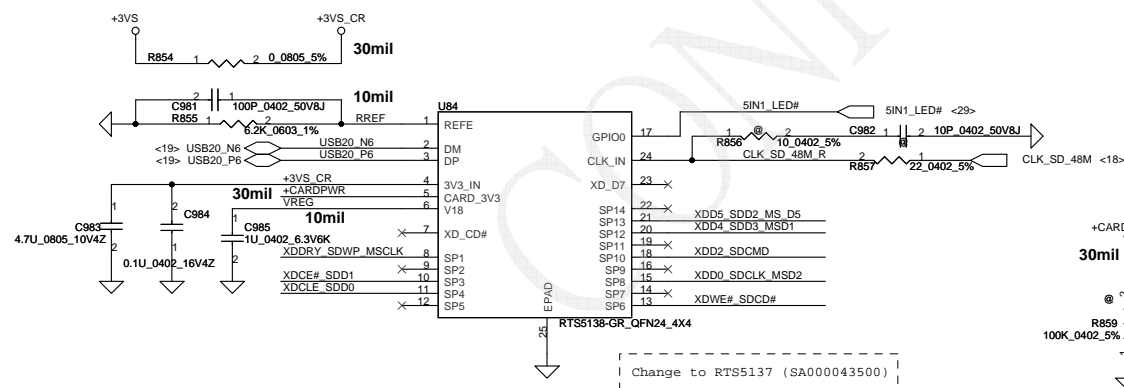
Card Reader RTS5138 / RTS5137
(only SD+MMC function)



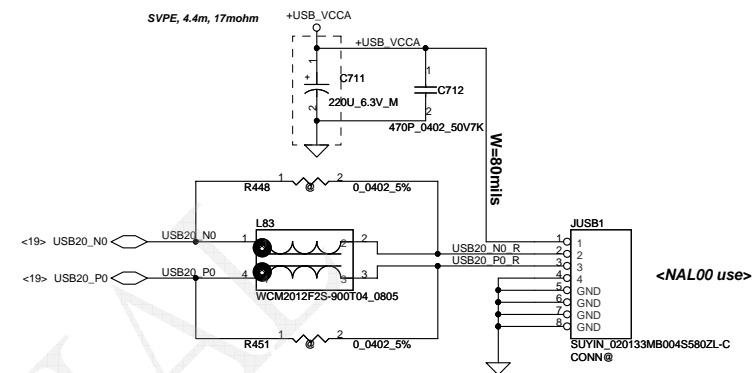
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Card Reader Connector



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					A	B	C
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USB20_N0_R 4

USB20_P0_R 3

+USB_VCCA_O 5

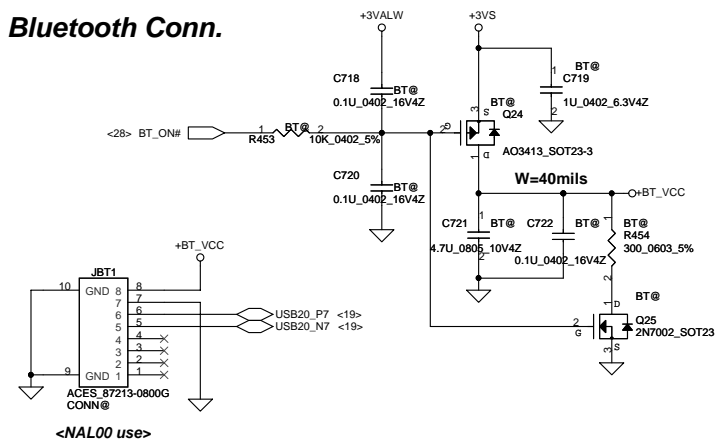
6

1

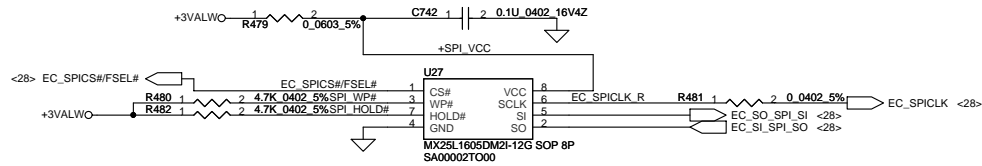
D10

PJUSB208_SOT23-6

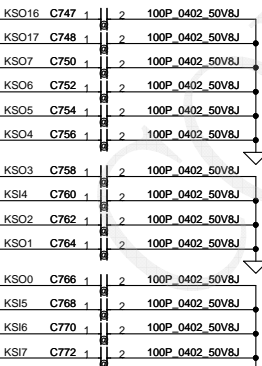
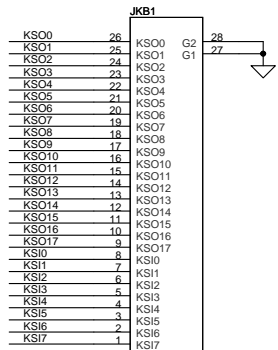
ESD Change P/N SC300000B00 For DVT



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Date:	Thursday, July 22, 2010	Sheet	27	of	45

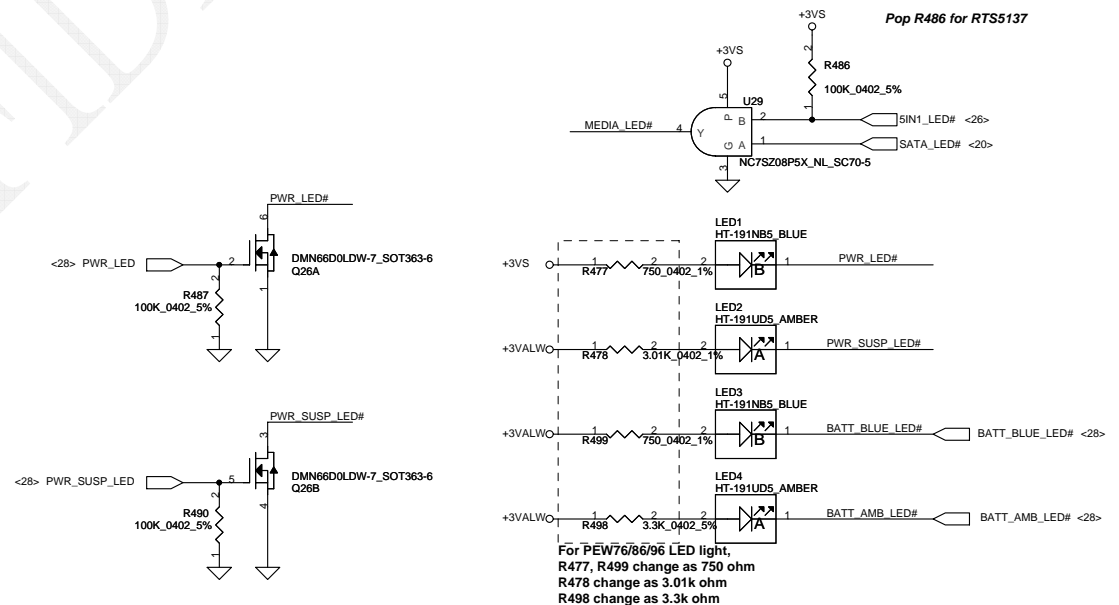
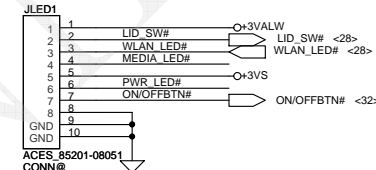
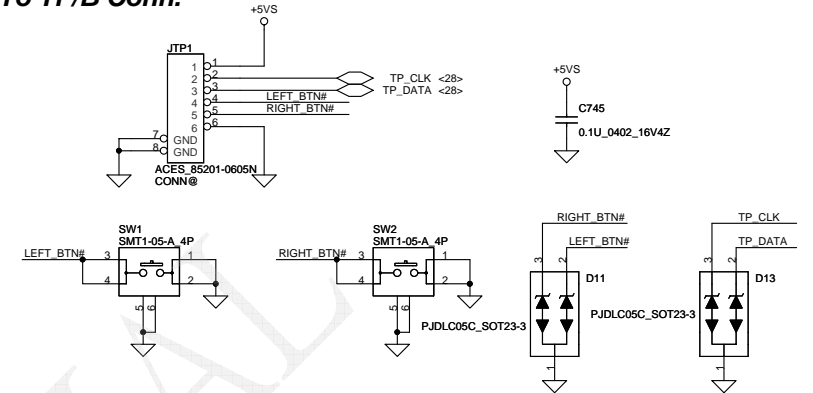


INT_KBD Conn.

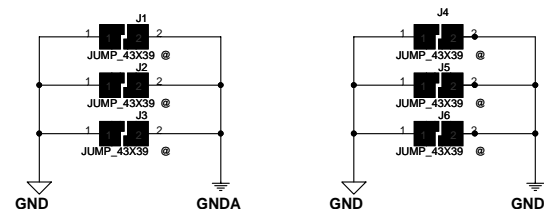
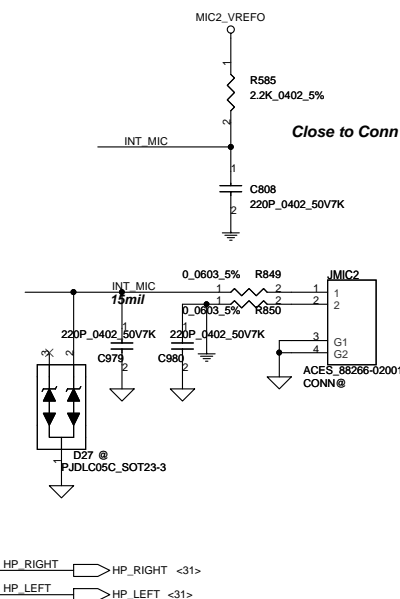
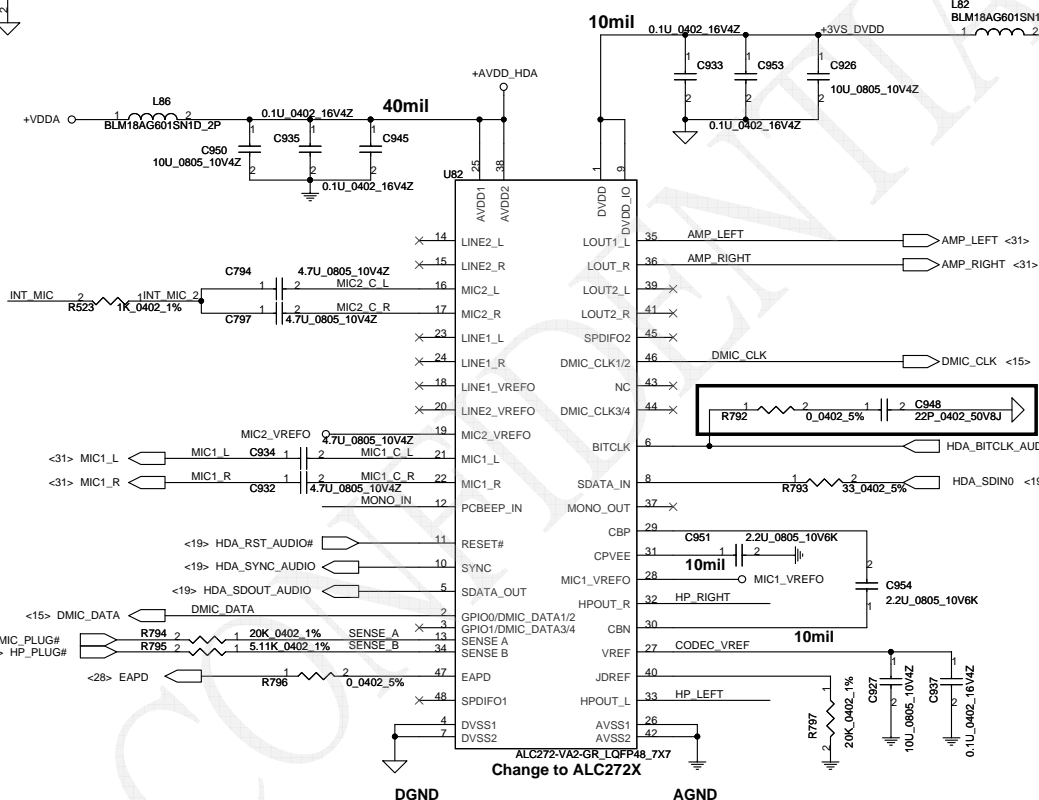


For PVT 0608 Unpop Cap.

To TP/B Conn.



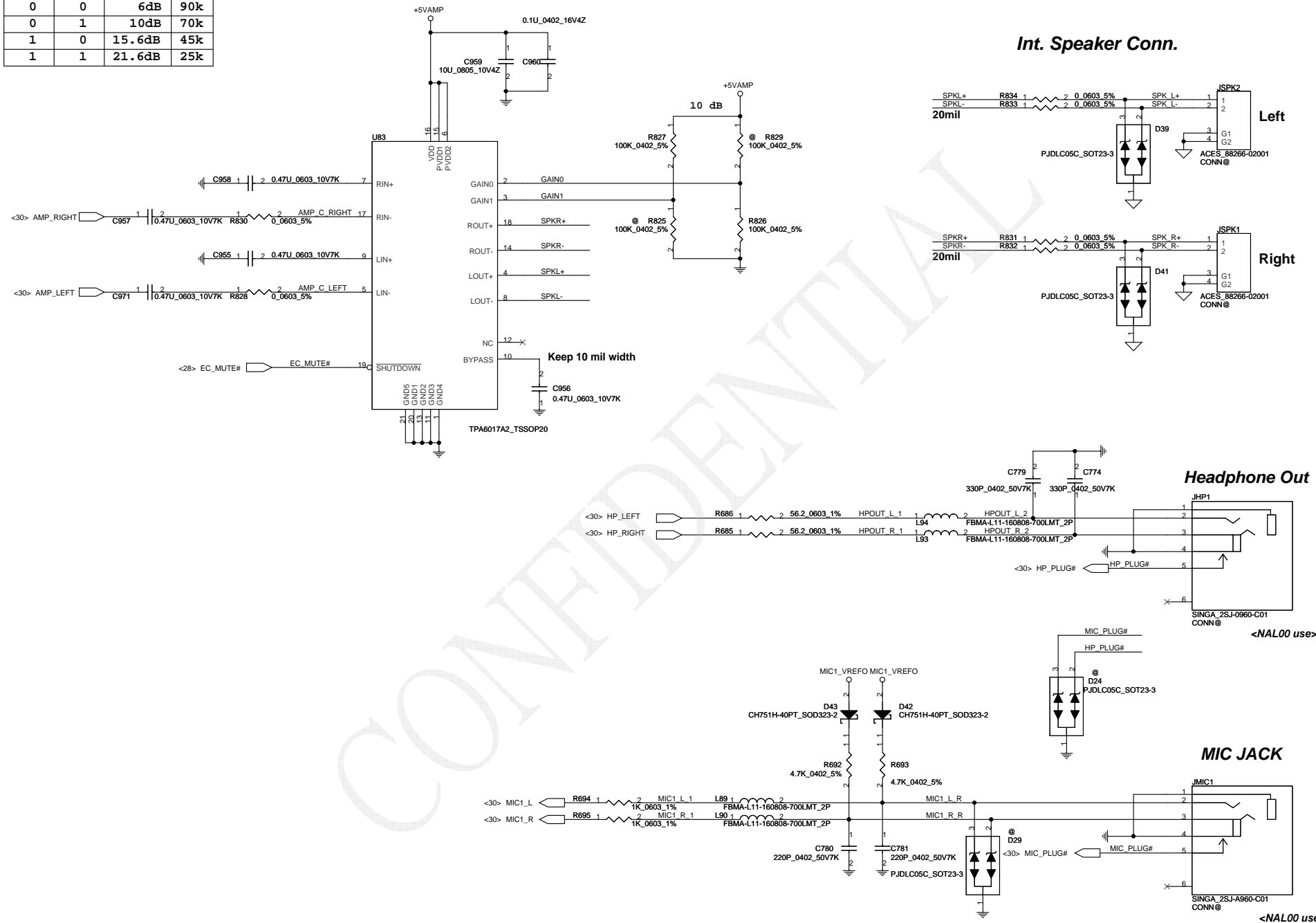
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K		
	5.1K	PORT-I (PIN 32, 33)	HP

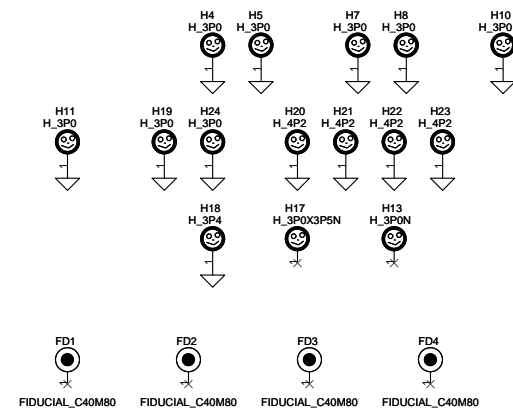
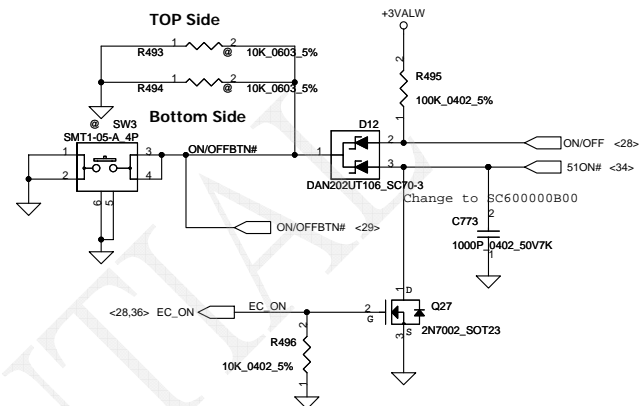
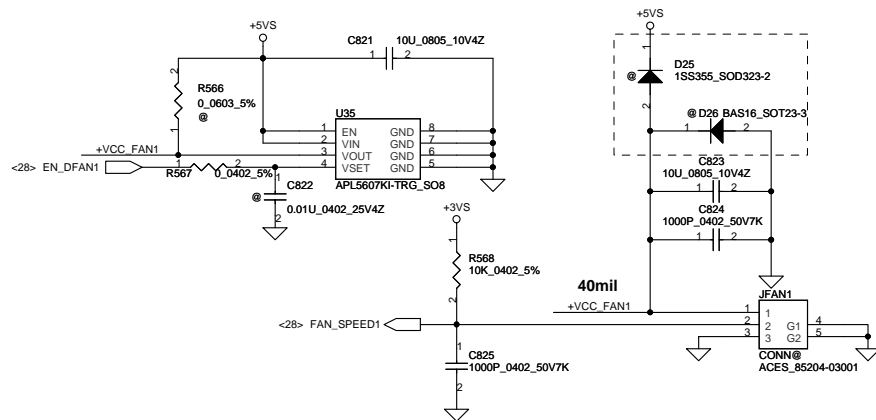
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				HD Audio Codec ALC272X	
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GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

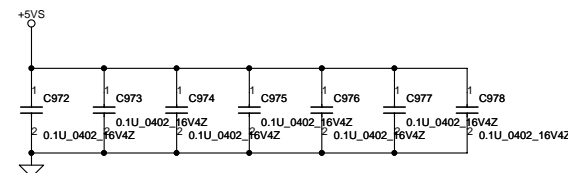
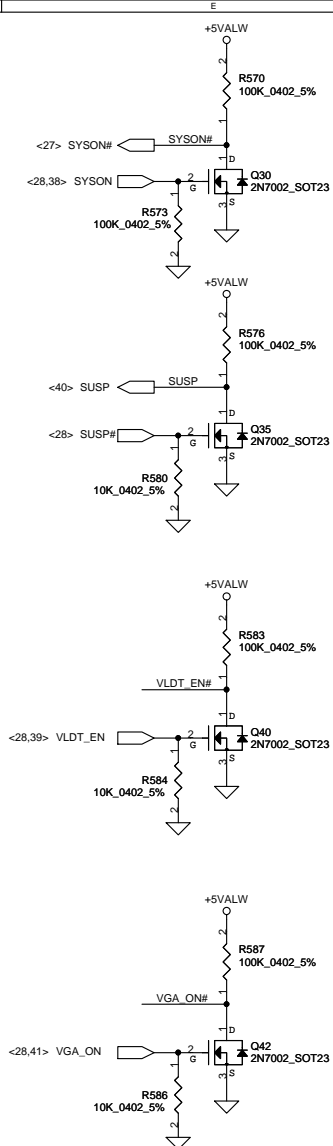
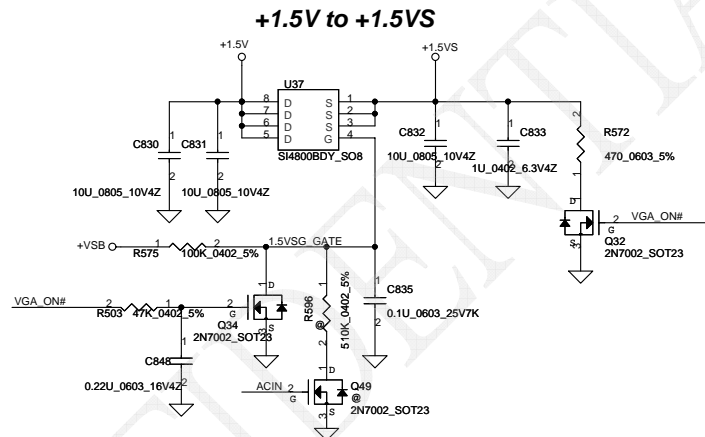
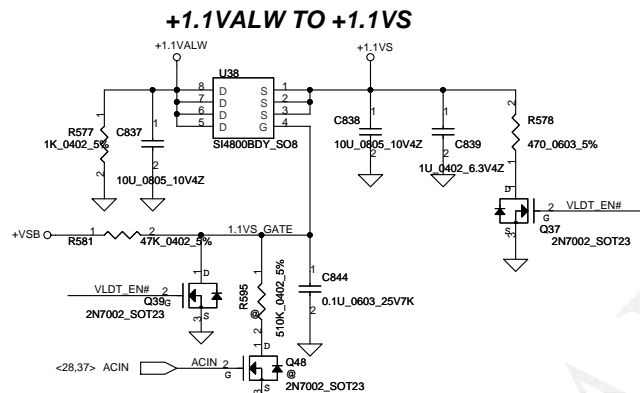
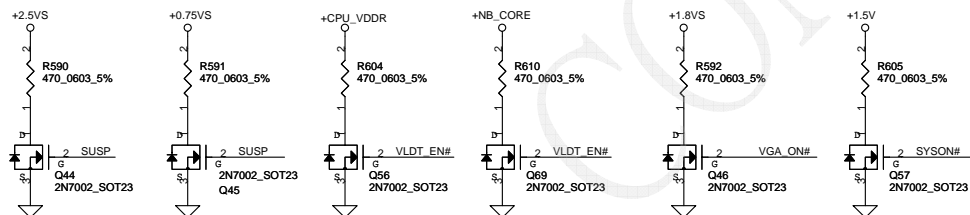
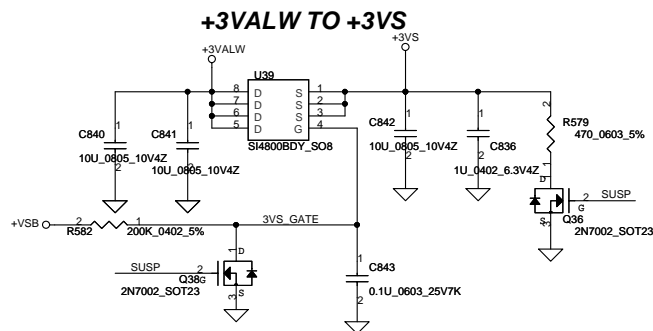
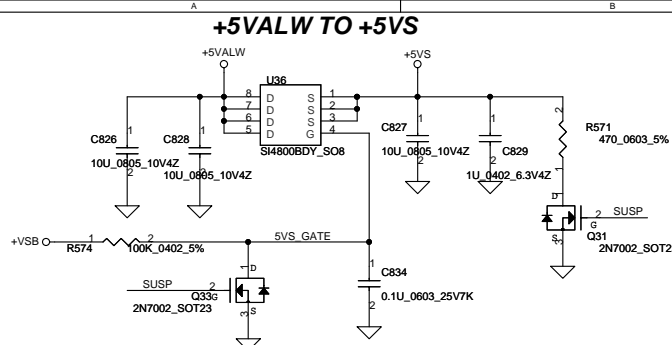


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ON/OFF switch **Power Button**



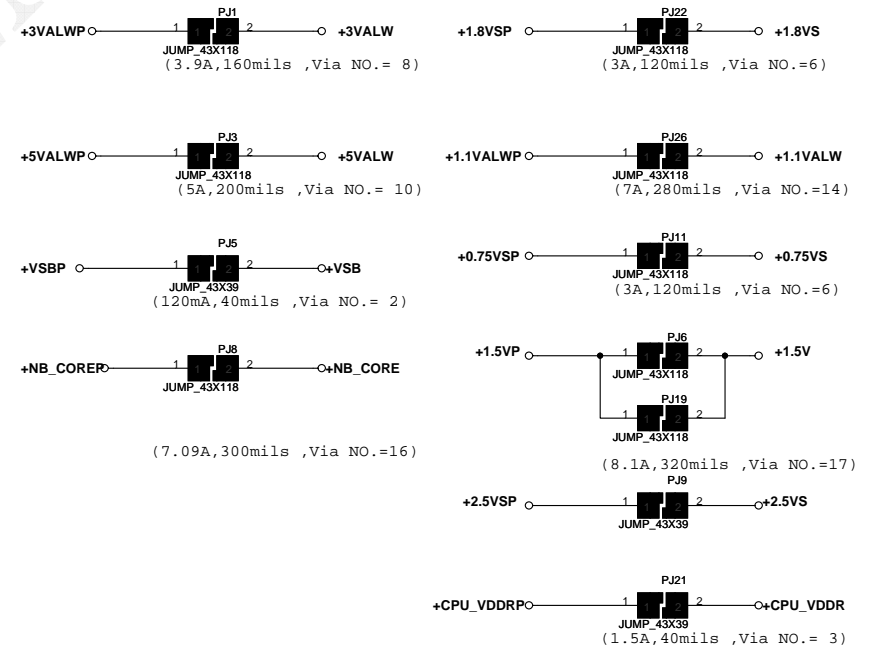
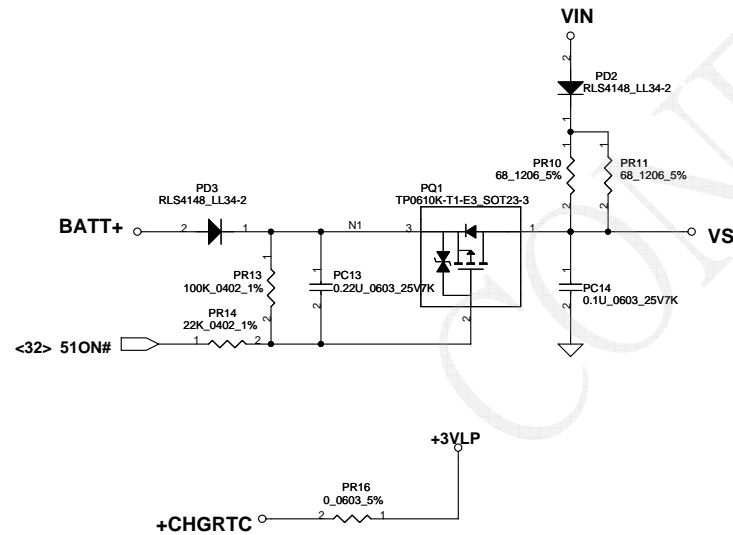
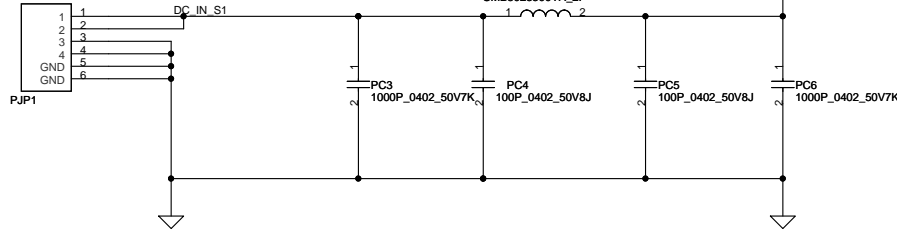
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						Document Number		Rev B	
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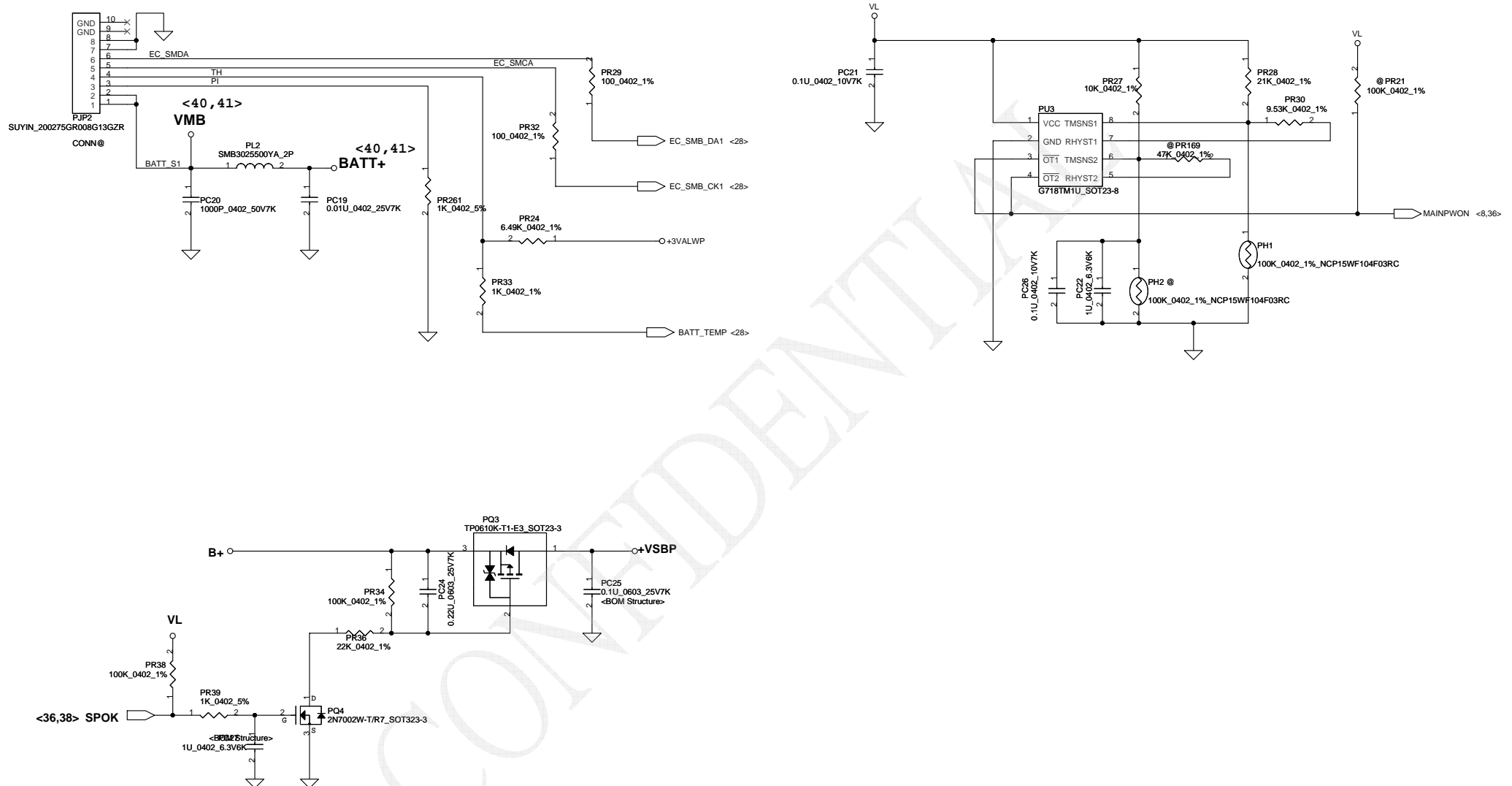
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DC-IN cable: DC301009W00 (Yellow)

SP02000GC00
ACES_90305-00441-001

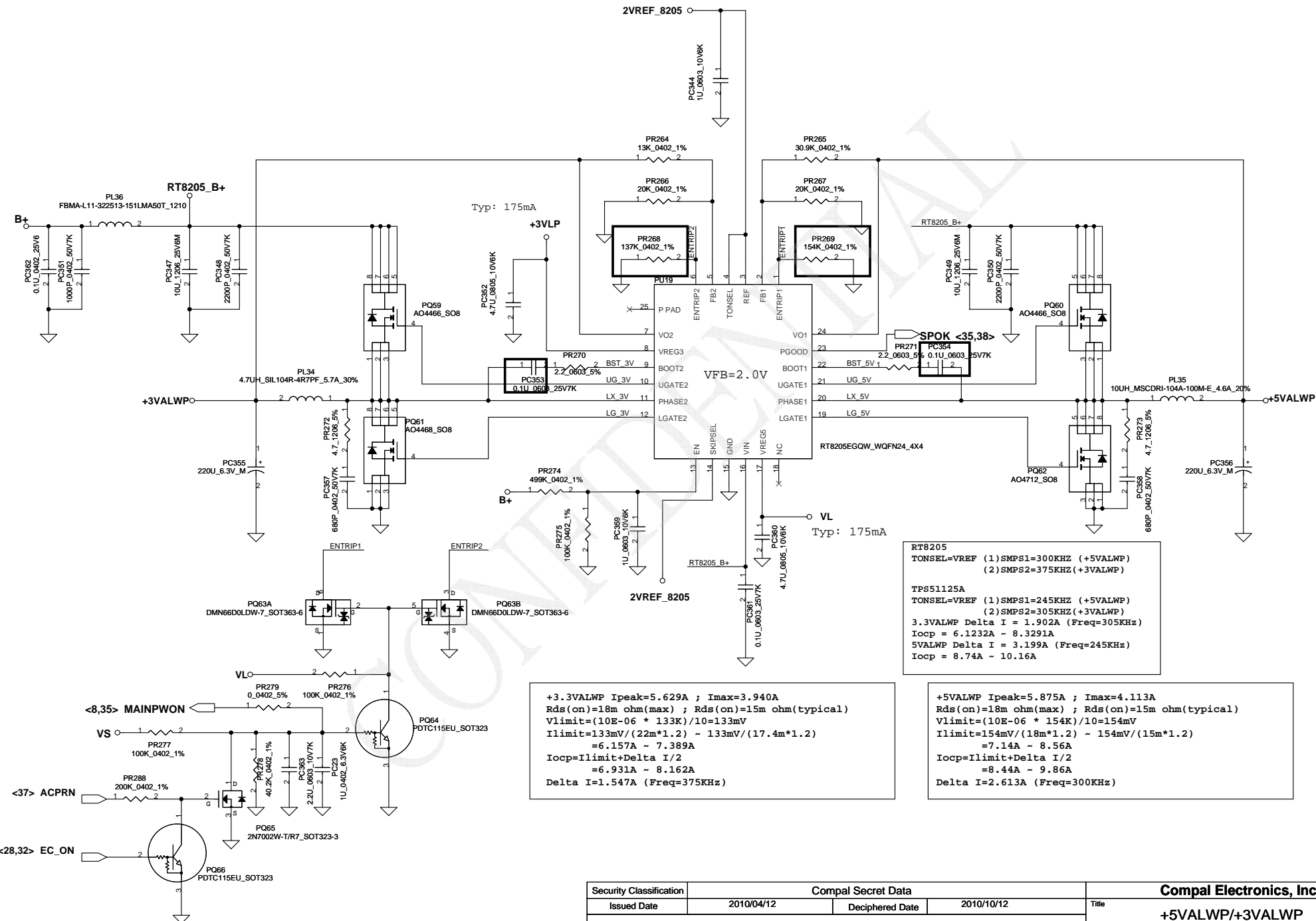


PH1 under CPU bottom side : Not SPEC, reference only!
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Note:
Use TPS51125 IC can remove RTC referenece LDO
Use TPS51427 IC must keep RTC referenece LDO



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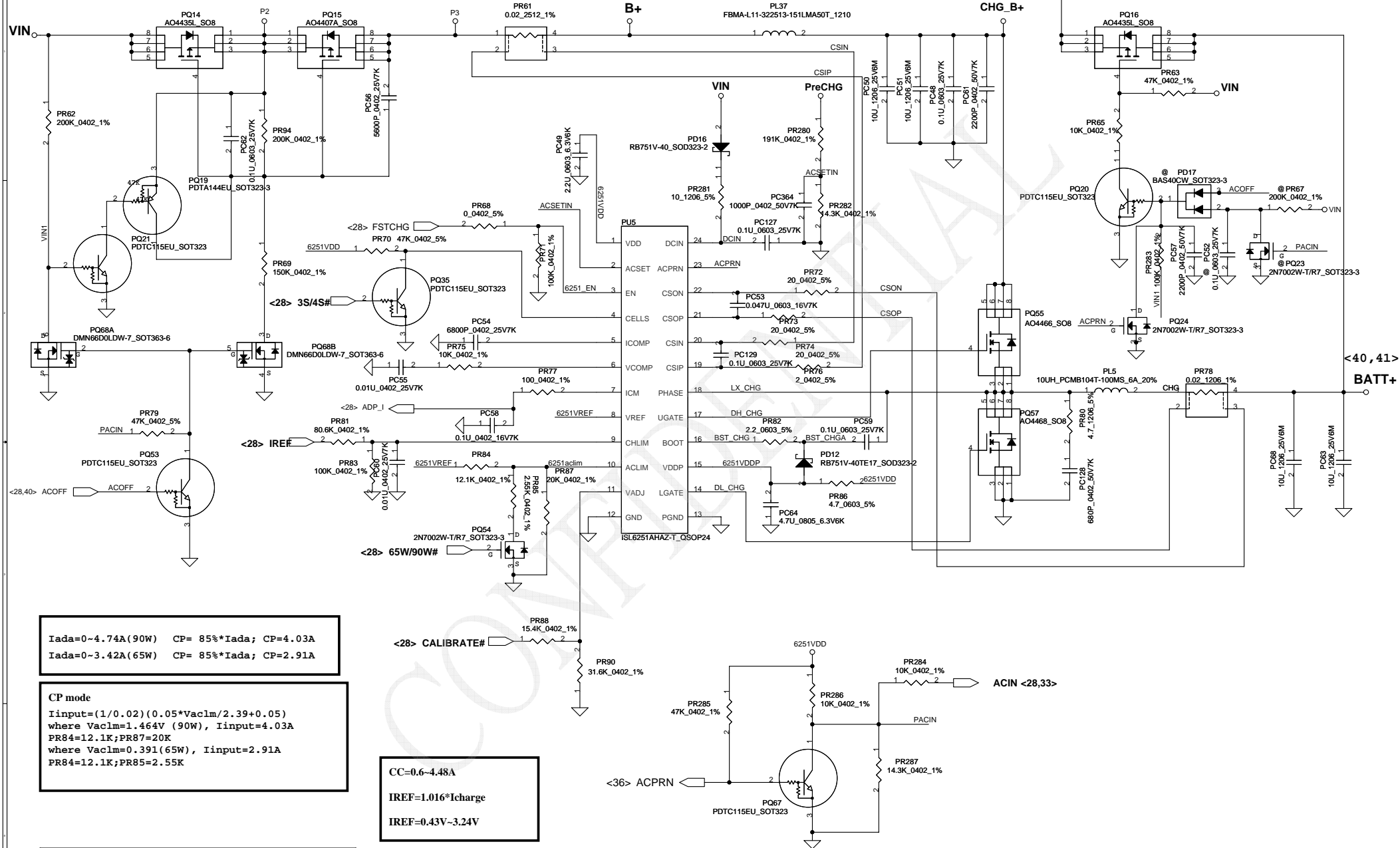
Iada=0~3.42A(65W/19V=3.421A)

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85*Iada ; CP = 2.91A

CP = 85*Iada ; CP = 4.07A



Iada=0~4.74A(90W) CP= 85*Iada; CP=4.03A

Iada=0~3.42A(65W) CP= 85*Iada; CP=2.91A

CP mode

Iinput=(1/0.02)(0.05*Vac1m/2.39+0.05)
where Vac1m=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vac1m=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K

CC=0.6~4.48A

IREF=1.016*Icharge

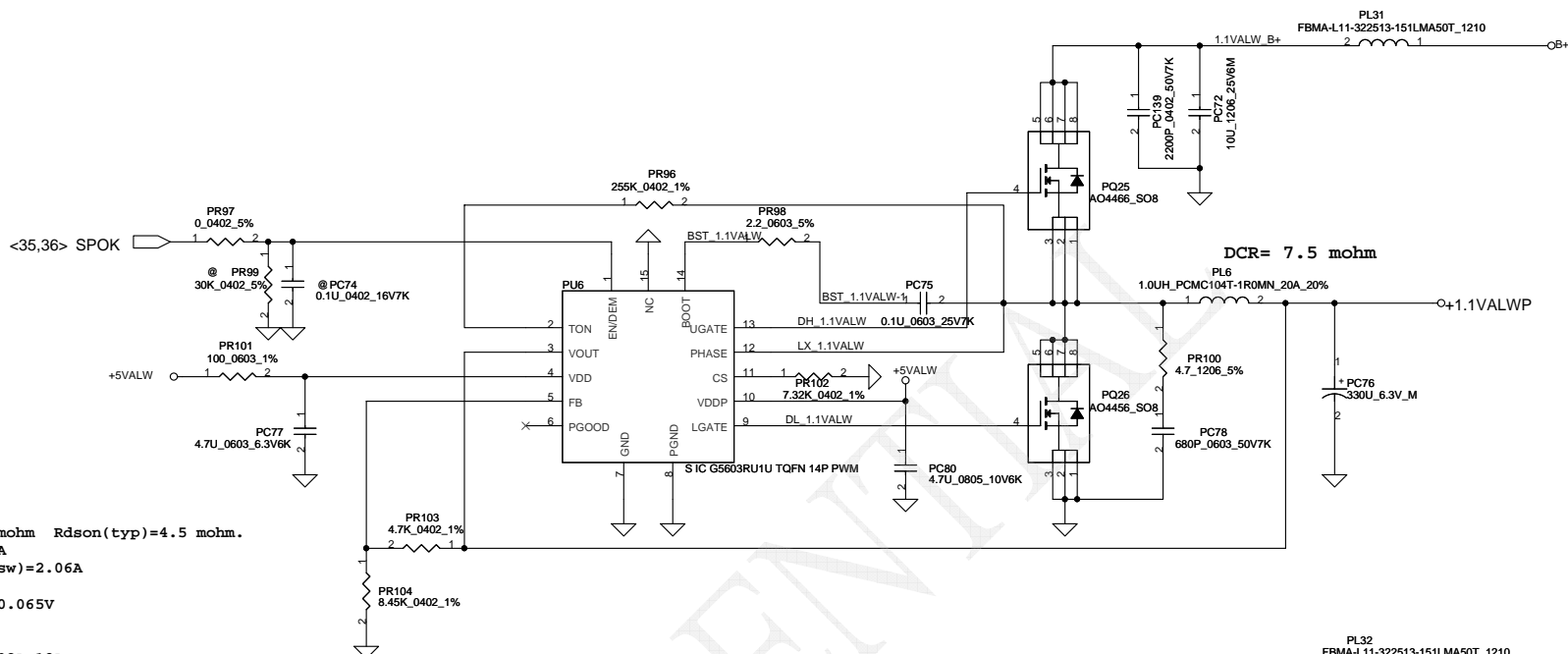
IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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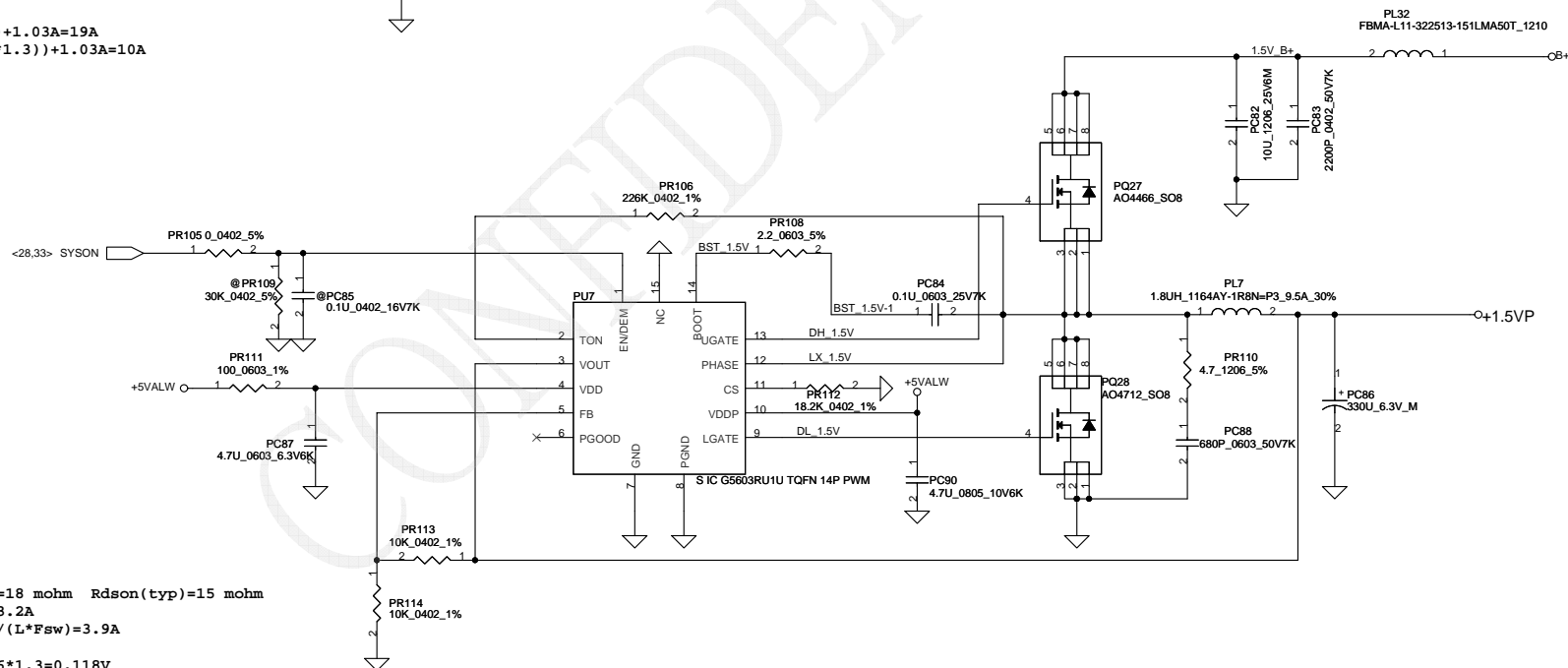
<Vo=1.1V> VFB=0.75V
 $V=0.75 \cdot (1 + 4.7K/10K) = 1.1V$
 $F_{sw} = 280KHz$

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
 $I_{peak} = 7.42A$, $I_{max} = 5.2A$, $I_{ocp} = 8.9A$
 $\Delta I = ((19-1.1) \cdot (1.1/19)) / (L \cdot F_{sw}) = 2.06A$
 $\Rightarrow 1/2 \Delta I = 1.03A$
 $V_{tripmax} = I_{ocp} \cdot R_{dson} = 8.9 \cdot 5.6 \cdot 1.3 = 0.065V$
 $R_{cs} = V_{trip} / I_{ocp} = 0.065V / 9uA = 7.2K$
 choose $R_{cs} = 7.32K$
 $I_{ocpmax} = ((7.32K \cdot 11uA) / 0.0045) + 1.03A = 19A$
 $I_{ocpmin} = ((7.32K \cdot 9uA) / (0.0056 \cdot 1.3)) + 1.03A = 10A$
 $I_{ocp} = 10A \sim 19A$



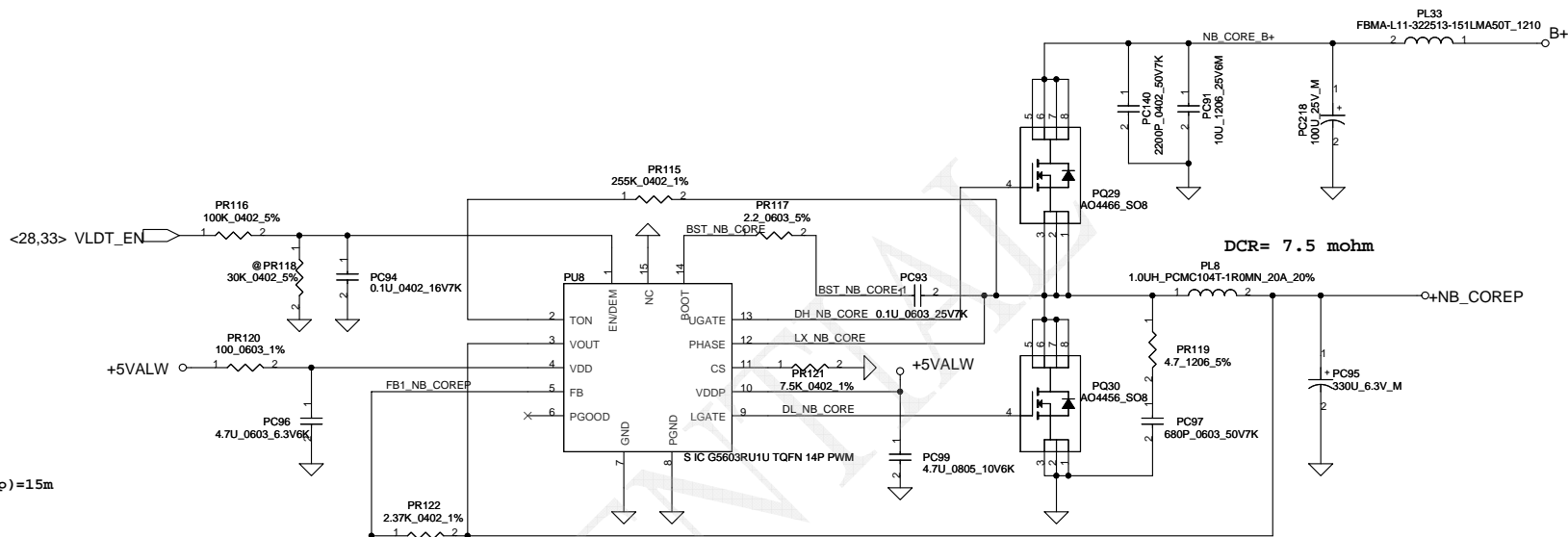
<Vo=1.5V> VFB=0.75V
 $V=0.75 \cdot (1 + 10K/10K) = 1.5V$
 $F_{sw} = 335KHz$

Cout ESR=17 mohm Rdson(max)=18 mohm Rdson(typ)=15 mohm
 $I_{peak} = 7A$, $I_{max} = 8.4A$, $I_{ocp} = 13.2A$
 $\Delta I = ((19-1.5) \cdot (1.5/19)) / (L \cdot F_{sw}) = 3.9A$
 $\Rightarrow 1/2 \Delta I = 1.95A$
 $V_{tripmax} = I_{ocp} \cdot R_{dson} = 16.2 \cdot 5.6 \cdot 1.3 = 0.118V$
 $R_{cs} = V_{trip} / I_{ocp} = 0.118V / 9uA = 13.1K$
 choose $R_{cs} = 13K$
 $I_{ocpmax} = ((13K \cdot 11uA) / 0.0045) + 1.95A = 32A$
 $I_{ocpmin} = ((13K \cdot 9uA) / (0.0056 \cdot 1.3)) + 1.95A = 18A$
 $I_{ocp} = 9.94A \sim 13.2A$

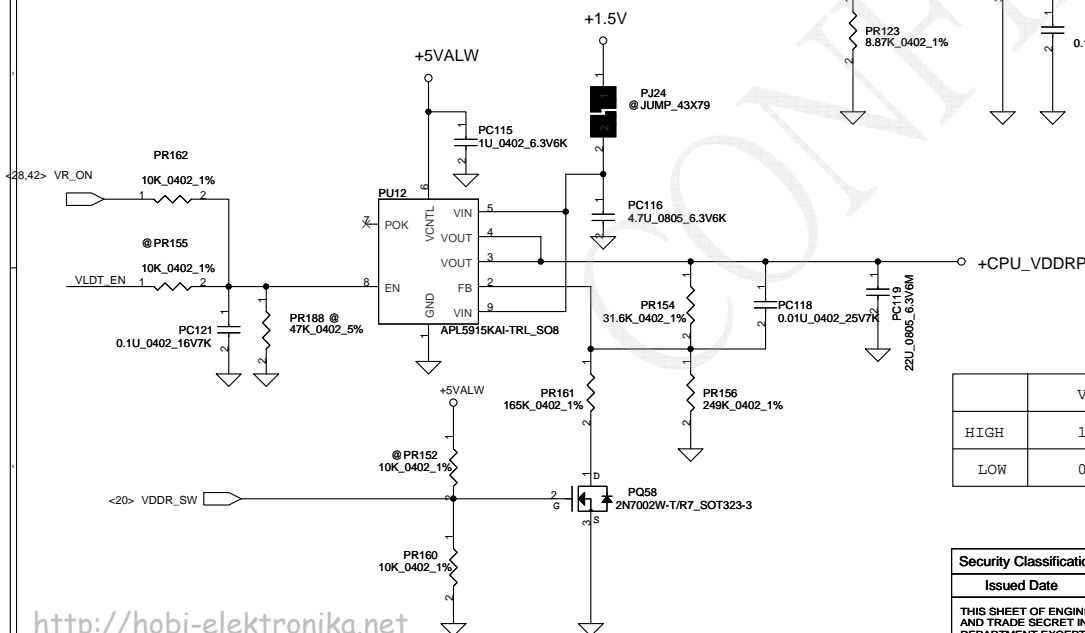


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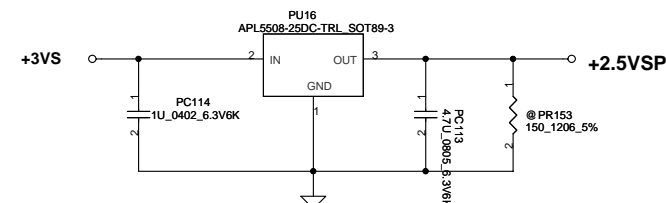
$<V_o=1.1V>$ $V_{FB}=0.75V$
 $V=0.75 \cdot (1+4.7K/10K)=1.1V$
 $F_{sw}=280KHz$
 $C_{out} ESR=15m \text{ ohm}$ $R_{dson(max)}=18m$ $R_{dson(typ)}=15m$
 $I_{peak}=7.6A$, $I_{max}=5.4A$, $I_{ocp}=9.2A$
 $\Delta I = ((19-1.1) \cdot (1.1/19)) / (L \cdot F_{sw}) = 2.06A$
 $\Rightarrow 1/2 \Delta I = 1.03A$
 $V_{tripmax} = I_{ocp} \cdot R_{dson} = 9.2 \cdot 5.6 \cdot 1.3 = 0.067V$
 $R_{cs} = V_{trip} / 9uA = 0.067V / 9uA = 7.44K$
 choose $R_{cs}=7.5K$
 $I_{ocpmax} = ((7.5K \cdot 11uA) / 0.0045) + 1.03A = 19.36A$
 $I_{ocpmin} = ((7.5K \cdot 9uA) / (0.018 \cdot 1.3)) + 1.03A = 10.3A$
 $I_{ocp}=10.3A \sim 19.36A$



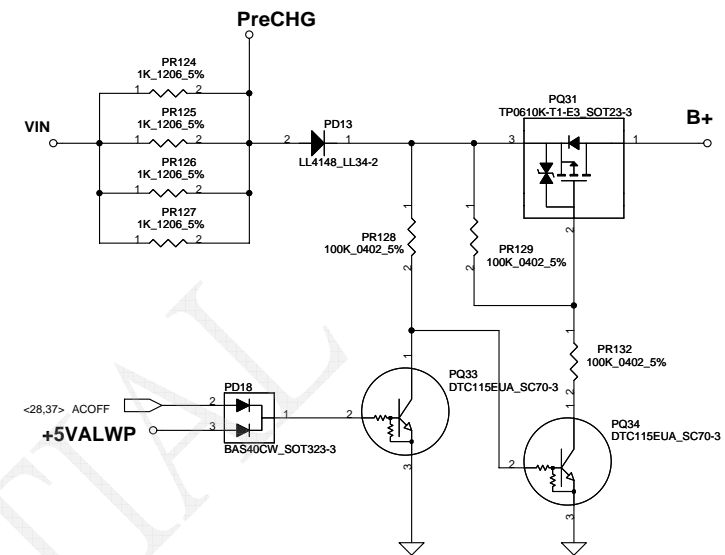
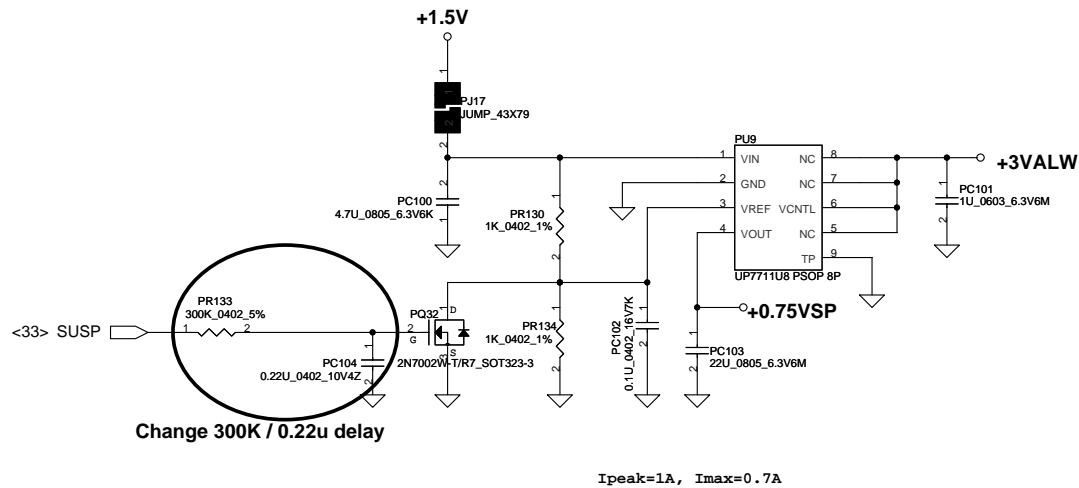
	POWER_SEL
HIGH	0.95V
LOW	1.1V

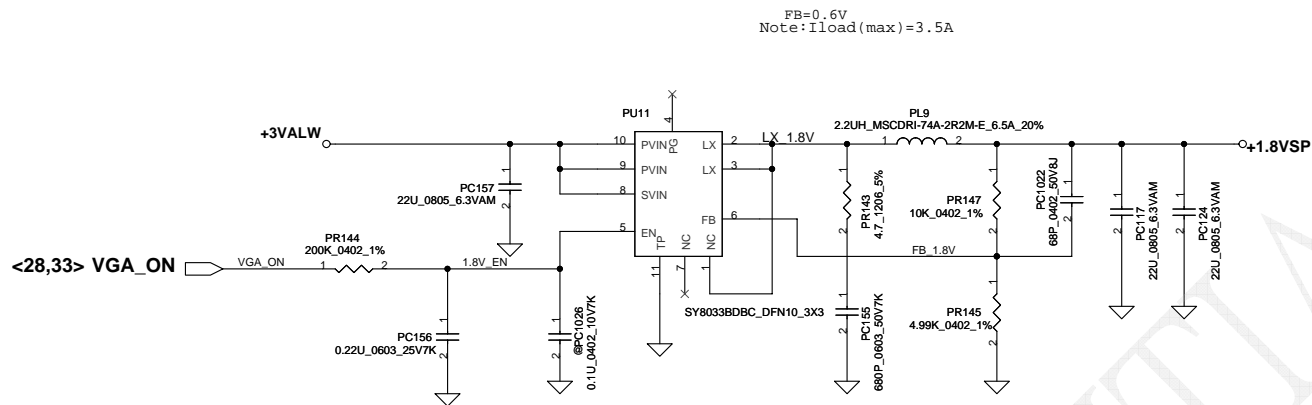


	VDDR_SW
HIGH	1.05V
LOW	0.9V



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify Pre-charger				Add PR279,PR288,PC57 Change PR285 100K to 47K Change PR287 20K to 14.3K Change PQ67 2N7002 to PDTCT115 Change PR62 47K to 200K Change PR79 22K to 47K Change PR283 0 to 100K	2010 0528	PVT
2	Meet common rule				Change PJ30 to PL36, PJ23 to PL37 Add PC361,PC362	2010 0602	PVT
3	HDMI test fail	5V voltage too low at test termial		36	Change PR265 from 30K to 30.9K	2010 0604	PVT
4	ESD test fail	ESD solution			Add PC22, PC23	2010 0608	PVT
5	EMI test fail	EMI solution			Enable 3V,5V,1.1V,1.5V,NB_CORE,CPU snubber	2010 0608	PVT
6	Power sequence tune			41	Change PR144 from 22K to 200K Change PC156 from 0.47u to 0.22u	2010 0609	PVT
7	Costdown	Costdown		38	Change PQ28 from AO4456 to AO4712 Change PR112 from 13K to 18.2K Change PL7 from 1.0uH to 1.8uH Change PQ61 from AO4712 to AO4468	2010 0617	PVT
8					PR268 from 133K to 137K PQ57 from AO4466 to AO4468		
9	For DDR voltage default/HW YC	DDR 2 need 0.9V, DDR 3 need 1.05V But DDR2 voltage is critical then DDR 3		39	Disable PR152 Enable PR160	2010 0705	Pre MP
10	Aprove 200MHz~220MHz/EMI Chris	EMI solution		37	Enable PR80, PC128 Change PR82 from 0 to 2.2	2010 0705	Pre MP
11	Add a bypass path/ESD Chris	ESD solution		35	Add PC26 near PC22	2010 0705	Pre MP
12							
13							
14							
15							
16							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
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05/10 First release

- 1. Change Cardreader chip (RTS5137/RTS5138)
- 2. ODD used to ODD sub/b
- 3. RTC Battery change (w/o charge)

06/11 PVT

- 1. P.28 Reserve R889 For EC_CLK, pop R851, unpop R852 For EC_SMBus leakage
- 2. P.26 Remove R853
- 3. P.28 project ID-->1 Board ID -->1, unstuff KSI, KSO Cap.
- 4. P.8 Change R41 as 31.6k ohm and R42 as 30k ohm for TSI

07/05 Pre-MP

- 1. P.19 Reserve R890 For MEM_1V5
- 2. P.28 Change R419 as 10 ohm For EMI

07/20

- 1. P.29 Change R477, R499 as 750 ohm; change R478 as 3.01k ohm; change R498 as 3.3k ohm for LED light

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